An Investigation of Input Protection for CDM Robustness in 40nm CMOS Technology

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Abstract - Adiabatic failures due to an initial peak voltage of VF-TLP measurements were observed at the input gate of a 40nm CMOS technology. Moreover, a correlation was verified between the failure current of the VF-TLP measurements and failure voltage of CDM testing. Through the transient analyses by a VF-TLP system, the performance of a diode-stack was better than that of SCRs as an input protection for CDM robustness.

I. Introduction

In advanced CMOS device applications beyond 45nm technology node, CDM ESD failures at thin gate oxide films are growing concerns. Although very fast transmission line pulsing (VF-TLP) systems are widely used to analyze device behavior during CDM ESD events [1-3], there is not enough understanding on the relationship between VF-TLP characteristics and CDM ESD performances. In this paper, a correlation between the failure current of VF-TLP measurements and failure voltage of CDM testing at the input gate is discussed by using a test-chip in a 40nm CMOS technology. Moreover, the performances of a couple of input protection devices with a low parasitic capacitance are evaluated for CDM robustness.

II. Experiment

A. Description of Test Structure

A 40nm CMOS test-chip in a QFP package with 208 pins was used in this work.

Figure 1 shows the equivalent schematic of the test structures, which have three types of primary protection devices and two types of secondary protection devices. Among all test structures, bonding pads, input inverters, power protection devices, and VDD/VSS bus lines were the same configurations. Also, the relative location of the primary and secondary protection devices was the same. Therefore, parasitic resistances, capacitances and inductances due to metal wirings were equal among all test structures. A breakdown voltage of the gate oxide film at the input inverter was about 4 V measured by a conventional 100ns TLP system. In these test structures, several combinations of the primary and secondary protection were evaluated.

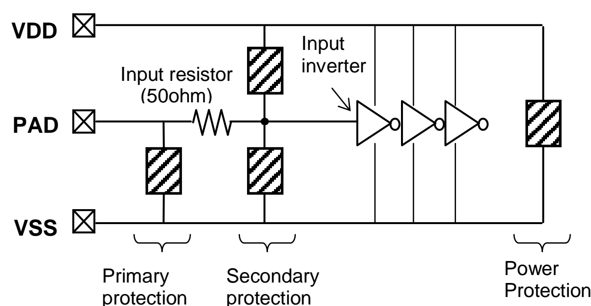

Figure 1: Equivalent schematic of test structures. All test structures have the same bonding pads, VDD/VSS bus lines, and power protection device, individually.

Figure 2 (a), (b) and (c), show equivalent circuits of the primary protection devices in the test structures, which are an NMOS-triggered SCR [4], a PMOS-triggered SCR [5] and a diode stack. All primary protection devices have the same reverse diode. Moreover, in the SCRs as shown in Figure 2(a) and (b), the layout and dimensions were the same except trigger elements, NMOS or PMOS. The area sizes of the p^+-anodes in the SCRs were nearly equal to that of the diode stack. All the primary protection devices have a parasitic capacitance of about 200fF including the reverse diode and metal wirings.

Figure 3 (a) and (b) show equivalent circuits of the secondary protection devices. In advanced CMOS processes, the voltage stress at the NMOS gate oxide

in inversion is the most critical [6]. Therefore, in the secondary protection devices, only the number of forward-biased diode between signal line and the V_{SS} was changed with considering of leakage current during normal operation and hot plugging. Both the secondary protection devices have the same p^+-anode sizes, which were about one tenth of that of the primary protection devices.

In this work, the analyses were focused on the positive polarity stress at the pad with respect to the V_{SS} in the VF-TLP measurement, and focused on the negative charged stresses in the CDM testing because these events were the most severe cases in this work.

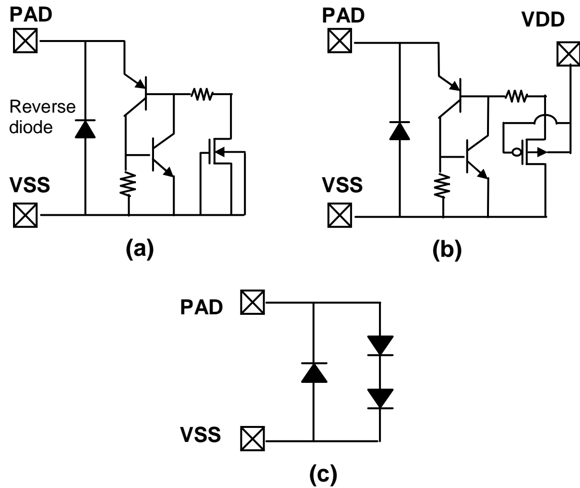

Figure 2: Equivalent circuits of primary protection devices in the test structures. (a): NMOS-triggered SCR, (b): PMOS-triggered SCR, (c): diode stack, respectively. Reverse diode was the same structure among all primary protection devices.

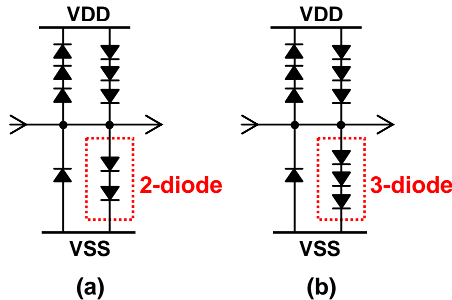

Figure 3: Equivalent circuits of secondary protection devices in the test structures. (a): 2-diode, (b): 3-diode, respectively. Only the number of forward-biased diode in the direction of Vss was changed.

B. VF-TLP Measurement

A VF-TLP system was used Model 4012 made by Barth Electronics. I-V characteristics were measured on 300mm wafers. Two pulse durations (T_d=1ns, 2ns) and three pulse rise times (T_{rise}=0.1ns, 0.2ns, 0.4ns) were applied. An averaging window to draw an I-V curve was 25-75% in the pulse duration as shown in Figure 4 and Figure 5 for example. The failure current, I_{t2}, was monitored at this averaging window. Also, an initial peak voltage, V_{peak}, in the voltage waveform was monitored. This V_{peak} is decreased by decreasing of the turn-on time of the protection devices, which is meaningful for CDM robustness.

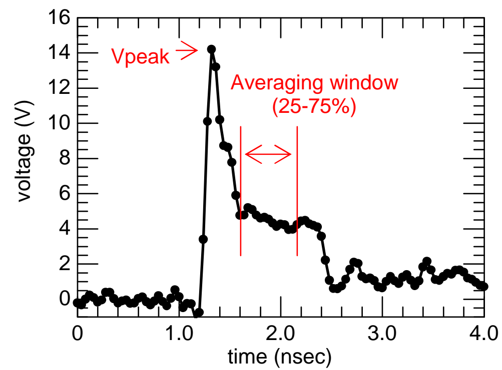

Figure 4: VF-TLP voltage waveform of NMOS-triggered SCR with 3-diode secondary protection. (Td=1ns, Trise=0.1ns)

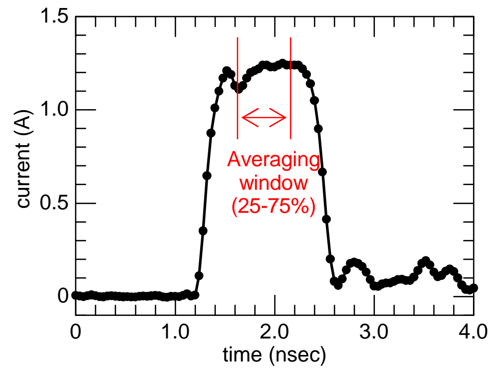

Figure 5: VF-TLP current waveform of NMOS-triggered SCR with 3-diode secondary protection. (Td=1ns, Trise=0.1ns)

Figure 6 shows an example of the I-V curve of the NMOS-triggered SCR with the 3-diode secondary protection at the averaging window. Although a slight increase of the DC leakage current occurs due to the gate oxides damage at the input inverter, it was regarded as a failure point in this work.

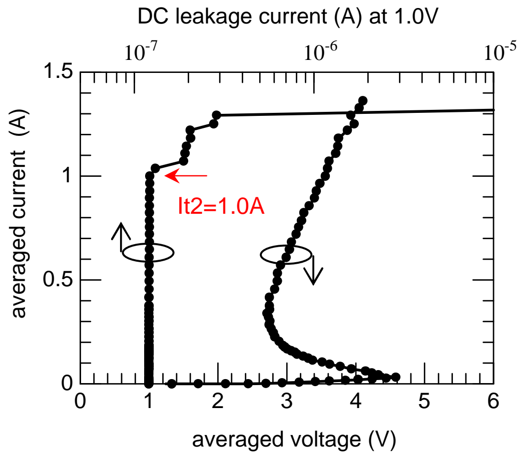

Figure 6: VF-TLP I-V characteristic at averaging window of NMOS-triggered SCR with 3-diode secondary protection. (Td=1ns, Trise=0.1ns)

C. CDM Testing

A CDM tester was used Model 550DFQM made by Tokyo Electronics Trading. The discharge waveforms of this tester were complied with JEDEC standard [7]. In this work, a direct contact discharge method with a relay after field-induced charging [8], was used although JEDEC standard defines the CDM testing as an air discharge method after field-induced charging. This is because the air discharge method has disadvantages from the point of reproducibility in the discharge waveforms [9]. Figure 7 shows the current waveforms by the direct contact discharge method in this work, whose reproducibility was better than that of the air discharge method as shown in Figure 8.

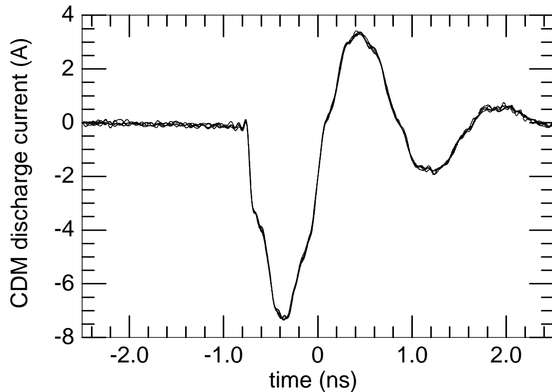

Figure 7: Current waveform in CDM testing by direct contact discharge method with a relay. Measuring oscilloscope bandwidth was 12GHz. (4pF module, -500V, 5 times)

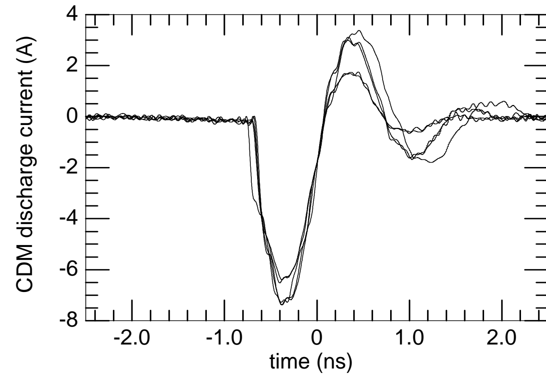

Figure 8: Current waveform in CDM testing by air discharge method. Ambient humidity was 45%RH. Measuring oscilloscope bandwidth was 12GHz. (4pF module, -500V, 5 times)

The voltage step of negative charging in the CDM testing was -50V. After the CDM stress, a slight increase of leakage current like several tens of nanoamperes was regarded as a failure as well as the VF-TLP measurements.

III. Results and Discussion

A. Results of VF-TLP measurements and CDM testing

Figure 9 and Figure 10 show relationship between I_{t2} and T_{rise} by the VF-TLP measurements. In the case of the 3-diode secondary protection as shown in Figure 9, the I_{t2} did not depend on the pulse duration, T_d, for all the T_{rise}. On the other hand, in the case of the 2-diode secondary protection, the I_{t2} did not depend on the T_d at only 0.1ns T_{rise}. These results mean adiabatic failures at the gate oxide of input inverter since the failure current level cannot be decreased with the pulse duration increasing. And these results show that the adiabatic failures are most remarkable at the fastest T_{rise} condition. In the case of the 3-diode, since the clamping voltage of the secondary protection is higher than that of the 2-diode, the adiabatic failures were occurred at all T_{rise} conditions.

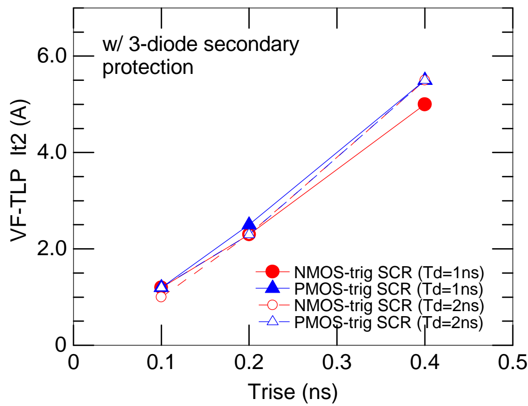

Figure 9: Relationship between It2 and T-rise by the VF-TLP measurements with 3-diode secondary protection.

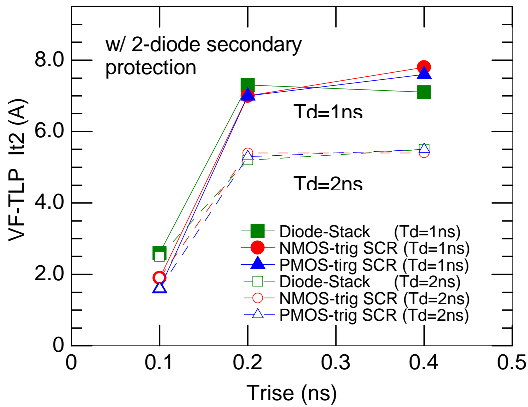

Figure 10: Relationship between It2 and T-rise by the VF-TLP measurements with 2-diode secondary protection.

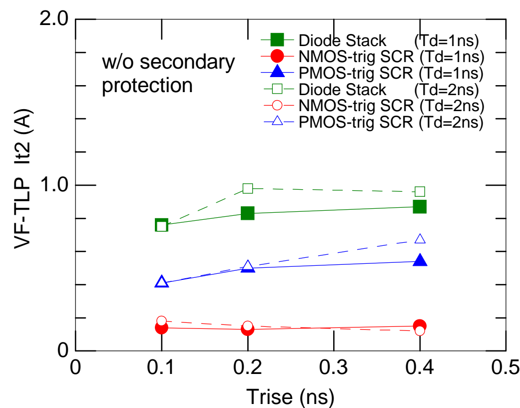

Figure 11: Relationship between It2 and T-rise by the VF-TLP measurements without secondary protection.

Figure 11 shows I_{t2} for the different T_{rise} of the test structures without the secondary protection and input resistor. Thus, the I_{t2} were decreased remarkably by using no secondary protection device. These results show that the secondary protection has a critical role to protect thin oxide films at the input gate of internal circuits.

Figure 12 shows the relationship between the applied pulse voltage, V_{pulse}, and the initial peak voltage, V_{peak}, for the NMOS-triggered SCR with the 3-diode secondary protection. The V_{peak} was the highest at 0.1ns T_{rise} and 1.0ns T_d. Thus, the highest V_{paek} was induced by the fastest T_{rise} and shortest T_d, because the primary protection device cannot turn on fully. From the view point of ESD protection design, the suppression of the adiabatic failure due to the V_{peak} at the input gate is effective for CDM robustness by using the optimum combination of the primary and secondary protection devices.

Figure 13 shows the relationship between the I_{t2} of the VF-TLP measurements and failure voltage of the CDM testing, V_{cdm}. As shown these results, a strong correlation was verified between the V_{cdm} and I_{t2} at the pulse condition of 0.1ns T_{rise} and 1ns T_d. The correlation factor of $V_{cdm}(V)$ / $I_{t2}(A)$ was about 200 ohm for all three types of primary protection and two types of secondary protection. This correlation factor may be changed by the changing of the test-chip configuration including the package. However, extensive studies are required on the correlation factor. It is meaningful that the diode stack as a primary protection device showed better CDM ESD robustness than that of the SCRs in this work.

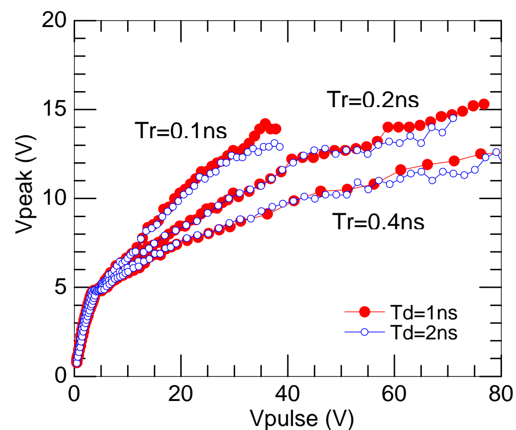

Figure 12: Relationship between Vpulse and Vpeak in the VF-TLP measurement of NMOS-triggered SCR with 3-diode secondary protection.

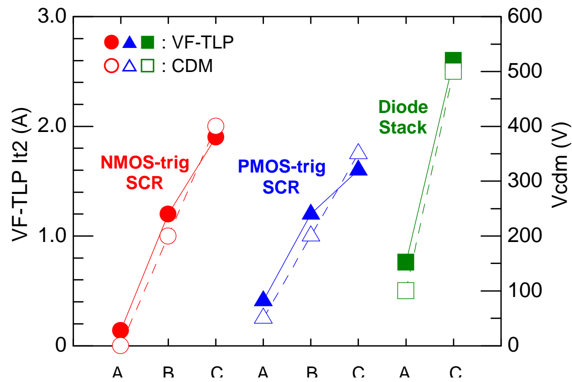

Figure 13: Relationship between It2 and Vcdm. It2 was measured at Td=1ns, Trise=0.1ns. (A: w/o secondary protection, B: w/ 3-diode secondary protection, C: w/ 2-diode secondary protection)

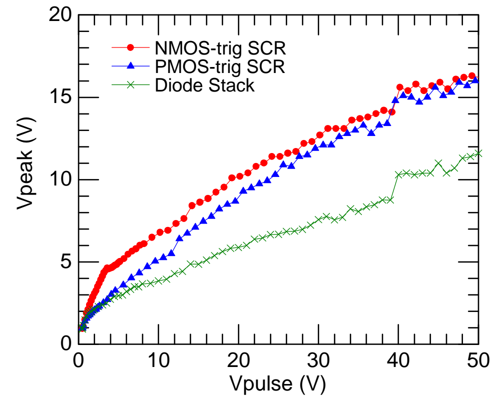

Figure 14: Relationship between Vpulse and Vpeak for different primary protection with 2-diode secondary protection. (Td=1ns, Trise=0.1ns)

B. Transient Behavior Analysis

As mentioned before, in the design of ESD protection for CDM robustness, to reduce the V_{peak} at the fastest T_{rise} and shortest T_d is important.

Figure 14 shows the relationship between the V_{pulse} and V_{peak} for the three primary protection devices at the fastest T_{rise} and shortest T_d. At the condition of low V_{pulse} below about 40V, the V_{peak} of the PMOS-triggered SCR was lower than that of NMOS-triggered SCR. However, with the V_{pulse} increasing the V_{peak} of the PMOS-triggered SCR became equal to that of the NMOS-triggered SCR. This result was due to the resistance of the metal wiring from the PNP base to the trigger element, NMOS or PMOS, because the V_{peak} depends on the impedance through the trigger element before the SCR turn-on. Therefore, in the design of SCRs, it is necessary the decreasing of the impedance of the triggering current pass for the CDM robustness.

Figure 15 shows I-V characteristics of the three primary protection devices at the averaging window. Although the on state resistance (R_{on}) of the primary protection of the diode stack was the largest among the three primary protection devices as shown in Figure 15, the V_{peak} of the diode stack was the lowest as shown in Figure 14.

Figure 16 shows the voltage waveform of the three primary protection devices at the averaged current level, 1A. The turn-on time of the diode stack was the fastest among three primary protection devices. Thus, faster turn-on time of primary protection device can be effective for the suppression of the V_{peak}.

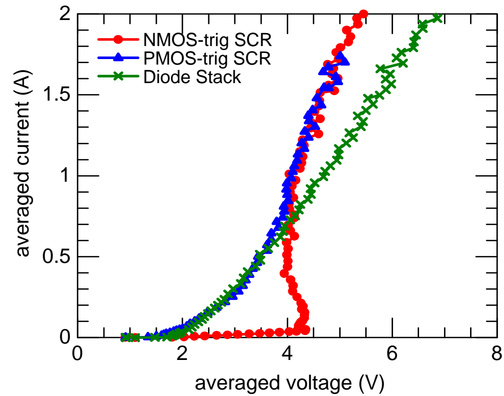

Figure 15: I-V characteristics at averaging window for different primary protection with 2-diode secondary protection. (Td=1ns, Trise=0.1ns)

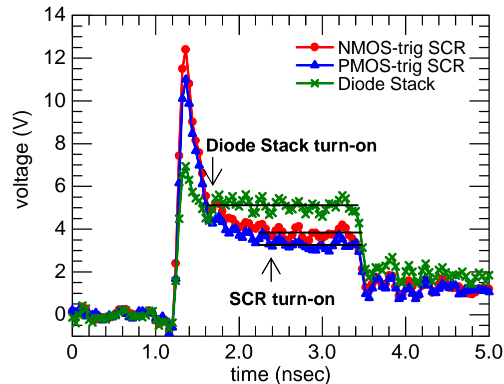

Figure 16: Voltage waveform at 1A averaged current level for different primary protection with 2-diode secondary protection. (Td=2ns, Trise=0.1ns).

C. DC Leakage Current

Although our experimental results show that the diode stack was superior to the SCRs for CDM robustness, the leakage current of the diode stack should be cared during normal operation at a high temperature. Figure 17 shows the leakage current of three primary protection devices without the secondary protection, which is compared with that of the 2-diode secondary protection. As a result, the leakage current of the diode stack was less than 10uA at 125℃, which means that this diode stack is usable for several 1.0V I/Os with considering the leakage current.

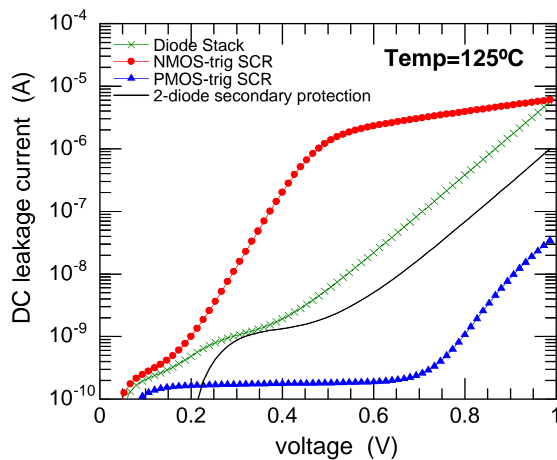

Figure 17: DC I-V characteristics between pad and Vss at high temperature (125ºC) for different primary protection devices without secondary protection. The result of 2-diode secondary protection was also showed for reference. Vdd was applied at 1.0V.

IV. Conclusions

A correlation between the VF-TLP measurements and CDM testing was investigated. As a result, adiabatic failures due to the input gate oxides were observed at the condition of the fastest pulse rise time, and the strong correlation was verified between the failure current of the VF-TLP measurements and the failure voltage of the CDM testing. Through our transient analyses, we think that the diode stack is most promising candidate as a local clamp for CDM robustness in 40nm CMOS technology and beyond.

Acknowledgements

The authors acknowledge the financial support of NEDO (New Energy and Industrial Technology Development Organization) through MIRAI project. The authors would also like to thank Akram Salman from Texas Instruments and Stephen Beebe from GLOBALFOUNDRIES for their kind assistance and mentoring.

References

[1] Horst Gieser and Markus Haunschild, "Very-fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model", EOS/ESD Symp. Proc., pp. 85, 1996.

[2] Junjun Li, Sami Hyvonen and Elyse Rosenbaum, "Improved Wafer-level VFTLP System and Investigation of Device Turn-on Effects", EOS/ESD Symp. Proc., pp. 331, 2004.

[3] Geert Wybo, Stefaan Verleye, Benjamin Van Camp and Olivier Marichal, "Characterizing the Transient Device Behavior of SCRs by means of VFTLP Waveform Analysis", EOS/ESD Symp. Proc., pp. 366, 2007.

[4] Yasuyuki Morishita, "New ESD Protection Circuits Based on PNP Triggering SCR for Advanced CMOS Device Applications", EOS/ESD Symp. Proc., pp. 6, 2002.

[5] Yasuyuki Morishita and Mototsugu Okushima, "A Low-Leakage SCR Design Using Trigger-PMOS Modulations for ESD Protection", EOS/ESD Symp. Proc., pp. 376, 2007.

[6] Adrien Ille, Wolfgang Stadler, Thomas Pompl, Harald Gossner, Tilo Brodbeck, Kai Esmark, Philipp Riess, David Alvarez, Kiran Chatty, Robert Gauthier, Alain Bravaix, "Reliability Aspects of Gate Oxide under ESD Pulse Stress", EOS/ESD Symp. Proc., pp. 328, 2007.

[7] JESD22-C101D, "Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components", JEDEC Solid State Technology Association, 2008.

[8] AEC-Q100-011 Rev-B, "Charged Device Model Electrostatic Discharge Test", Automotive Electronics Council, 2003.

[9] Tilo Brodbeck, Kai Esmark, Wolfgang Stadler, "CDM Tests on Interface Test Chips for the Verification of ESD Protection Concepts", EOS/ESD Symp. Proc., pp. 1, 2007.