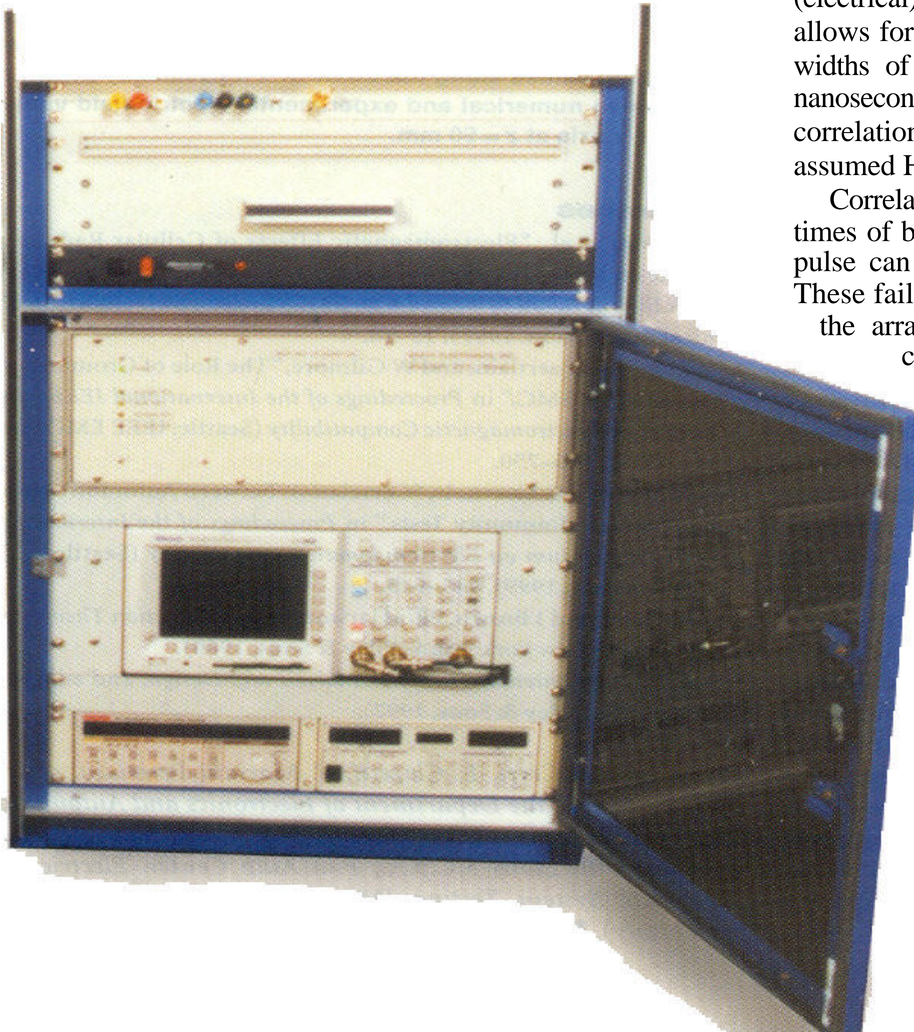
Transmission-Line Pulse ESD Testing of ICs: A New Beginning

Leo G. Henry, Jon Barth, Koen Verhaege, and John Richner

A new technique for accurately tracking leakage currents has emerged.

The integrated circuit (IC) industry has been using transmission-line pulse (TLP) testing to characterize on-chip electrostatic discharge (ESD) protection structures since 1985. This TLP ESD testing technique was introduced by Maloney and Khurana as a new electrical analysis tool to test the many single elements used as ESD protection structures.[1,2] Since then, the technique has been shown to be most useful as a means for reducing the design cycle time for these protection circuits.[3,4]

A TLP tester employs a rectangular pulse with energy ranges similar to those used in human body model (HBM) ESD qualification testing.[5] The pulse width of the TLP is chosen to provide the same current-amplitude damage levels (electrical) as is found in HBM ESD stress testing. This allows for correlation between TLP (with rectangular pulse widths of 75-200 nanoseconds) and HBM (with a 150-nanosecond, double-exponential pulse width).[6] The correlation is established through the TLP current and the assumed HBM peak current, i.e. V_{hbm} [V] + 1500O.[7,8]



Correlation is further achieved by comparing the rise times of both systems, because the rise time of either threat pulse can cause significant differences in device failures. These failures are due to the ?V/?t effects in the layout and the arrangement of components in the ESD protection circuit. These considerations allow a one-to-one correlation between the two methods and, hence, the means to correlate the electrical damage of the device under test (DUT) and the physical location of the failure site.[9,10]

The traditional way to represent the behavior and response of the protection element is to show a current-voltage (I-V) characteristic curve and use the It_2 position as the point of failure (see Figure 1).[11,12] This I-V curve shows avalanche voltage, V_{av} (also referred to as the turn-on voltage, Vt_1); the snapback voltage, V sp; the snapback region (also referred to as the impedance of the structure); and the second breakdown point (Vt_2, It_2). A literature review reveals that few have measured the leakage after each pulse discharge, and it appears that even fewer have consistently published in-situ leakage evolution measurements.[13] This article provides a basic review and discusses why leakage evolution during TLP ESD testing must be monitored. It also includes an

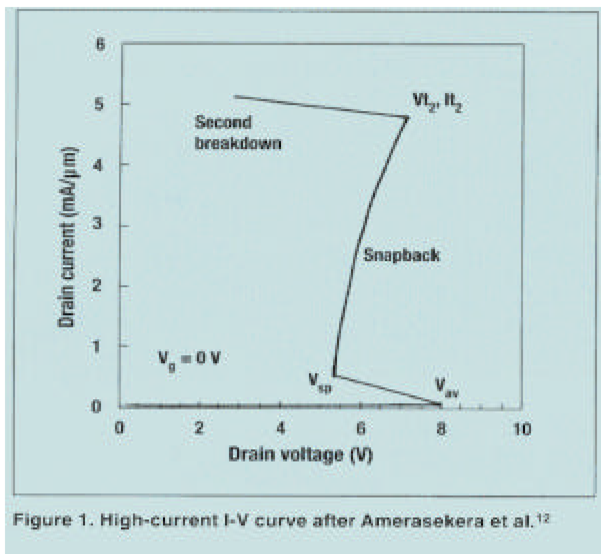


Figure 1. High-current I-V curve after Amerasekera et al.[12]

elegant plot that shows both the TLP I-V and the leakage evolution data.

Introduction to TLP

A TLP simulator (tester) uses very short ESD pulses (nanosecond pulse widths and rise times). By using a flattop pulse, both the current through the DUT and the voltage across the DUT can be measured accurately to provide the DUT's I-V characteristics. HBM testers, however, are designed to simulate (or attempt to simulate) real-life HBM to qualify ICs to specified immunity levels.[5,14] Initially, HBM stress- testing results were also used for analysis of ESD designs to determine whether they met the desired level of immunity. As TLP testing has become more widely available to IC manufacturers, it has quickly replaced HBM for design analysis.

In-house-built TLP test equipment systems have been used for many years, but undefined measurement errors required considerable expertise to interpret the data from each different system.[1,2,15] However, TLP testing was the only method that could provide the dynamic electrical characteristics of each ESD protection design at high pulse currents. As ESD designers provided data showing fairly good relationships between TLP and HBM testing, TLP testing became more widely used, and its test data became more accepted as an effective design analysis tool.

In contrast, traditional HBM ESD testing for qualification requires the use of a discharge circuit, a 1500-.Q resistor and 100-pF capacitor connected in series.[5] The resulting stress pulse is a double-decaying exponential waveform, with most standards specifying a rise time of 2-10 nanoseconds. The ESDA standard rise-time specification for the HBM test pulse has been 2-10 nanoseconds for many years, but most HBM testers built for testing 256 pins or more have a rise-time pulse of 9-10 nanoseconds.[16]

TLP Basics

In the TLP tester setup, a transmission line is charged and discharged to produce a narrow (75-200-nanosecond) rectangular pulse, which is then applied to the ESD protection structure connected to the pins of an IC.[2,3] The TLP tester is capable of providing an I-V characteristic curve and therefore can be regarded as a pulse-curve tracer. The pulse has an energy content similar to that used in HBM ESD stress testing.[17] TLP-pulse stress testing to failure levels provides a peak current comparable to the peak HBM current that fails the DUT. It is important to note that with an ordinary curve tracer, the much higher amount of energy associated with the longer (microsecond) pulse widths dissipated in the ESD protection circuit limits the current to a small fraction of what the same circuit is capable of handling with shorter ESD pulses.

When TLP testing>is used in its primary function as a design tool, its analytical capabilities allow testing each element used in protection structures to determine individual pulse-current capability and dynamic I -V characteristics. This function provides a designer with data indicating how each will perform in the final circuit assembly. Knowing the current path a stress pulse takes through an ESD protection structure and its dynamic impedance at I and V values enables optimal design of each element. Each diode, transistor, resistor, and metal interconnection can be TLP

A transmission line is charged and discharged to produce a narrow rectangular pulse.

stress-tested individually to provide a library of component size, layout, and optimum construction to be used in 'a complete ESD protection circuit.

Constant-Current TLP Systems. Traditional or classical TLP systems use a shunt resistor to ground and a 500-1000-O series resistor to the DUT to provide a constant current source. The shunt resistor is typically 53-56 O to offset the 50-O mismatch introduced by the parallel path including the DUT (see Figure 3). This is defined as a TLP-500 or TLP-1000 system, depending on the impedance. It is a constant-current system. Note, however, that in most systems, the series resistor uses ranges from 450 to 500 O.[5] Because both the DUT impedance and the tester source impedance determine the voltage and current parameters at the DUT for any pulse source voltage, the impedance of a TLP system is defined as the source impedance that the DUT sees.

Constant-Impedance TLP. The TLP system used has a constant impedance of 50 O up to the DUT (see Figure 2). This is defined as a TLP-50 system because it uses a constant impedance of 50 O throughout the system and the pulse is not degraded. This TLP system produces a pulse from the standard 50-O transmission-line source, followed by a matched 50-O attenuator to absorb reflections from the DUT. From there, the pulse travels through the rise-time filters, the coaxial voltage and current sensors, a switch to a pA-meter, and then on to the DUT.

The operation of the 50-O transmission line, high-voltage

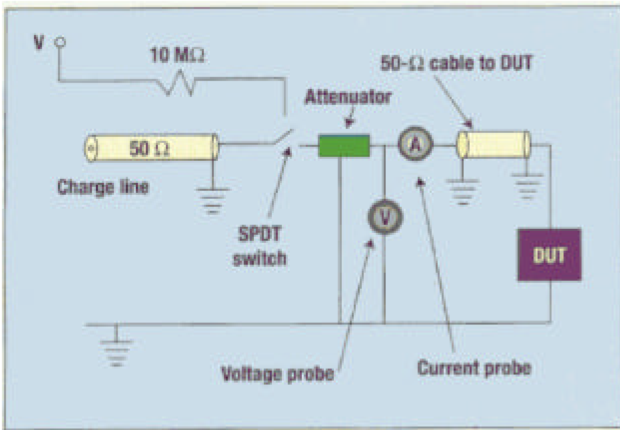


Figure 2. TLP-50: a constant-impedance 50-Ω TLP system.

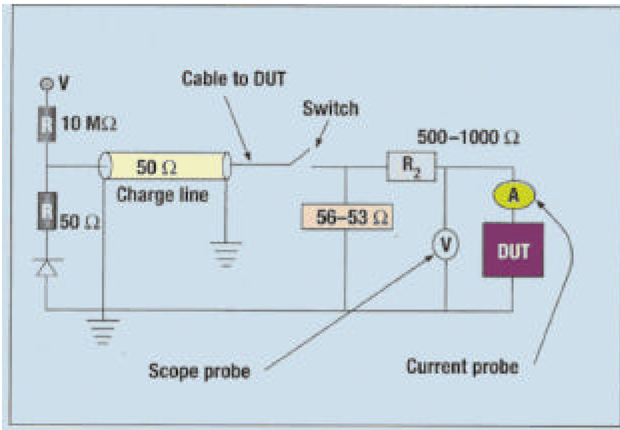


Figure 3. TLP-500: a constant-current 500-Ω TLP system.

(HV) power supplies and switch used to generate rectangular (or square) pulses has been explained in a number of other sources and so is discussed only briefly here.[18]

The advantage of maintaining a 50-O constant-impedance system for the pulse travel through the system is shown in the rise time of the TLP pulse. Although the HV switch provides the fundamental limit to the pulse rise time, the reflection losses among all coaxial connections, including the transmission lines and the switch, further limit the usable test-pulse rise time.[19]

TLP Measurements

The simplest TLP systems can provide the current-voltage (I- V) data of the ESD protection circuits, which can be displayed either on the tester or can be plotted on a computer using plotting software. Such a plot allows accurate measurements of both the voltage across the device and the current through the device by averaging the digitized data for some length of time near the end of the pulse (pick-off points range from 50 to 95% of the pulse width).

TLP testing is a significant improvement for ESD design because it provides an analysis tool unavailable with HBM. Moreover, TLP can measure and display the dc leakage-current evolution of the DUT, that is, the leakage measurement after each pulse, rather than the measurements at the beginning and end of the stress test. Adding a dc leakage-current measurement of the DUT after each test pulse provides additional insight into minute changes in damage to the protection or core circuits, which is unavailable without this measurement. The dc leakage-current data combined with the I -V data provide electrical indications of where damage begins, and how rapidly it can evolve from soft to hard failure.9 These I-V and leakage data on a device are defined as the electrical damage signature.

Measurements were made using the constant-impedance TLP system, defined earlier as TLP-50 (see Figure 2). The circuit arrangement shown in Figure 2 allows the DUT to be momentarily disconnected from the pulse source after each pulse with a coax switch, so that the DUT can be connected to a dc voltage source and pA-meter. During this time, a dc leakage measurement at the selected dc voltage (usually V_{dd}, the positive end of the power-supply voltage, ± 10%) was made after every test pulse with the DUT in situ. The leakage current measurement was then plotted with the I-V plot against the measured pulse current (the current through the DUT). The constant-impedance system allows both the DUT response and DUT leakage measurements to be made either when testing socketed devices or when TLP stress testing on wafers.

Stress Testing

The most common way to stress test single-element or

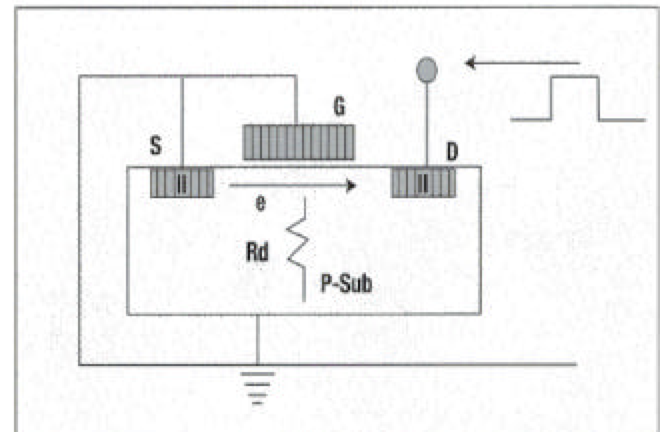


Figure 4. Basic schematic showing the single-element protection structure being stress-tested.

multiple protection structures is to use wafer-level stress

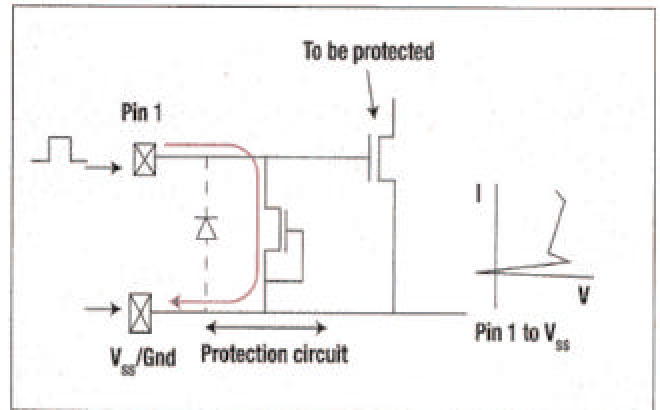


Figure 5. The protection structure on a wafer with the first protected core element.

testing. In general, for meta-oxide semiconductor (MOS) devices, the drain (collector) is stress tested while the gate, the source (emitter), and the substrate are tied to ground. Figure 4 illustrates a single-element structure under stress. Figure 5 shows the path of the current through the protection structure. The resulting I-V characteristic curve is shown on the right (for example, pin 1 to V_{ss}, the negative end of the power-supply voltage).

I.V and Leakage Evolution Plots

Figures 6-8 represent several characteristic responses from a typical nMOS device. In all three figures, the plots on the right represent the I-V characteristic curve using the bottom x axis (device voltage) and the vertical y axis (device current). The plots on the left indicate leakage evolution. After the collection of each I-V data point, a simple dc leakage measurement is done on the DUT. This dc leakage value (top x axis) is obtained for a specified dc bias (e.g. V_{dd} + 10%) and is then plotted on the y axis as a function of the stress parameter (the TLP pulse current). Each leakage evolution plot, therefore, represents the leakage change (if any) at each incremental pulse current, with the DUT bias remaining constant throughout all leakage measurements.

In Figure 6, using the I-V curve only, the structure shows no problems up to what appears to be the It_2 point (where Vt_2 = 9.9 V). In this figure, the I-V plot indicates an It_2 point at 2.2 A. The figure also shows that the leakage (top horizontal scale) changes from 10^{-10} to 10^{-6} A, a change of 4 orders of magnitude. These electrical data indicate a failure, which appears to be catastrophic. Here, the leakage failure coincides with the It_2 point, which is typically regarded as the catastrophic second breakdown failure point.

In Figure 7, the I-V curve on the right shows the normal turn-on or trigger at 16.5 V (lower horizontal scale), the regular snapback (to 9.5 V), and the linear impedance region. However, the leakage evolution curve (left) shows a soft failure mechanism at 4 A (vertical scale). The leakage indicated by the top horizontal scale changes from 10^{-10} to 10^{-9} A, and appears before the hard failure at 8.6 A (vertical scale). Some- thing has changed in the device, and it is safe to say that the structure is damaged. Such electrical signatures are usually termed soft failures.

Without this leakage evolution, there would be no indication from the I -V plot that something had changed in the device. If a change is undetected, this can lead to field returns, which are typically designated as latent failures. Because the leakage was not detected, the device likely passed the qualification test. Determining the leakage evolution allows analysts to stop the stress at the soft-failure point to perform physical failure analysis.[9] This allows identification of the physical location of the start (weakest point) of the failure, particularly if multiple failed locations are possible or expected.

Based on the I-V curve alone, the structure shows no sign of a problem (see Figure 8). The trigger point occurs at 40 V, and the snapback is approximately 40 V. However, the leakage evolution continues to change from nanoamps to milliamps, which is several orders of magnitude. Again, without the insitu simultaneous collection of data and plotting of both the I-V and leakage evolution, the indication of damage is hidden.

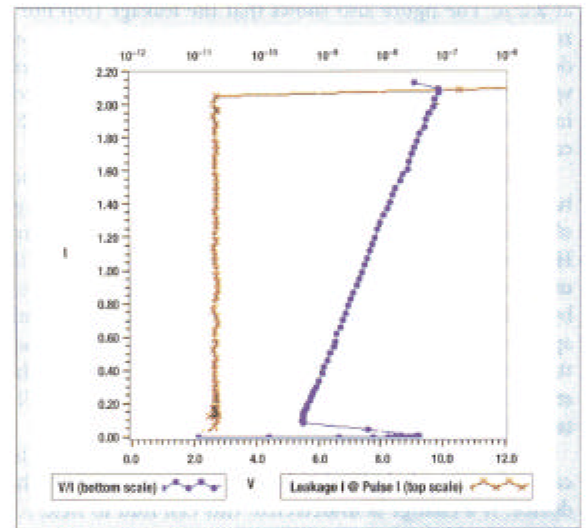


Figure 6. I-V plots showing It_2 failure coinciding with high-leakage failure.

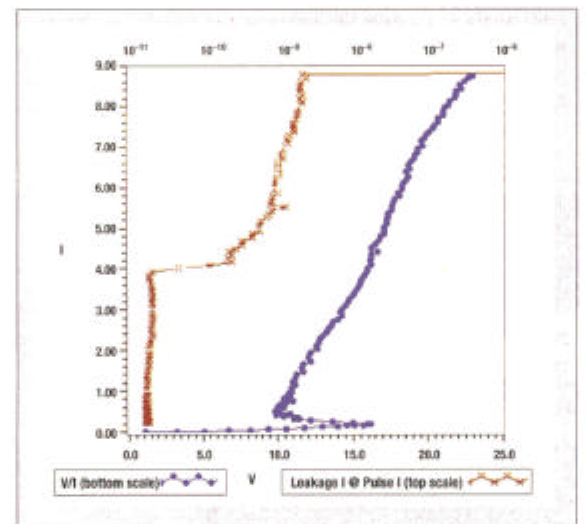


Figure 7. Soft failure followed by a hard failure.

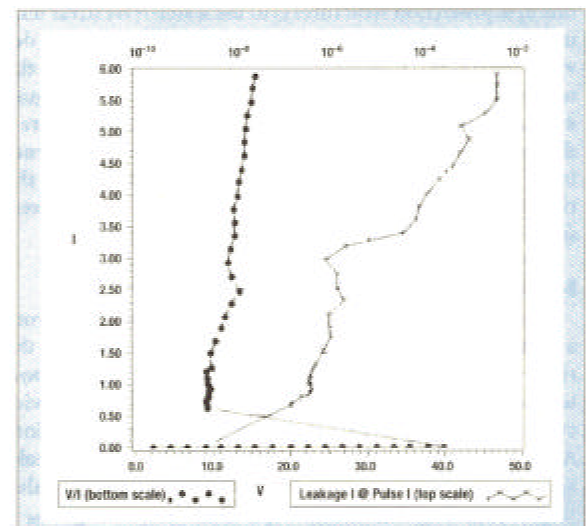


Figure 8. Complete TLP data set showing a continuously changing leakage evolution. The leakage data indicate a bad device or design, while the I-V behavior is much less conclusive.

Conclusion

This article describes an improved transmission-line pulse measurement technique and shows that the new technique accurately tracks the leakage current evolution in the device. This tracking is in addition to the traditional current and voltage measurements of the DUT.

TLP ESD stress testing of single ESD protection structure elements provides the detailed data a designer needs to determine soft failures. TLP can be regarded as an engineering and design tool, whereas the HBM stress test is a qualification tool that provides levels of threshold failures (that is, classes such as 1, 2, 3, etc.) which are related to increases in voltage- failure levels. The pulse width and rise times of the TLP were chosen to provide the same current-amplitude damage level (electrical) as is found in HBM ESD stress testing.

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References

1. T Maloney and N Khurana, "Transmission Line Pulsing Techniques for Circuit Modeling of ESD Phenomena" in *Proceedings of the EOS/ESD Symposium* 7, (Minneapolis, MN: ESD Association: 1985): 49-54.
2. N Khurana, T Maloney, and W Yeh, "ESD on CHMOS Devices-Equivalent Circuits, Physical Models and Failure Mechanisms" in *Proceedings of IEEE IRPS* (Orlando, FL: International Reliability Physics Symposium, 1985): 212.
3. S Beebe, "Methodology for Layout Design and Optimization of ESD Protection Transistors" in *Proceedings of the EOS/ESD Symposium* 18 (Orlando, FL: ESD Association, 1996): 255.
4. C Russ et al" "Non-Uniform Triggering of ggNMOSt Investigated by Combined Emission Microscopy and Transmission Line Pulsing" in *Proceedings of the EOS/ESD Symposium* 20 (Reno, NV: ESD Association, 1998): 177-186,
5. *ANSI/EOS/ESD-S5.1-1999,* "ESD Sensitivity Testing (Human Body Model)," ESD Association, Rome, NY,
6. DG Pierce et al., "Electrical Overstress Testing of a 256K UVEPROM to Rectangular and Double Exponential Pulses," in *Proceedings of he EOS/ESD Symposium* 10 (Anaheim, CA: ESD Association, 1988): 137,
7. G Notermans, P de long, and F Kuper, "Pitfalls When Correlating TLP, HBM and MM Testing," in *Proceedings of the EOS/ESD Symposium* 20 (Reno, NV: ESD Association, 1998): 170-176.
8. A Amerasekera et al., "An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes" in *Proceedings of the EOS/ESD Symposium* 12 (Lake Buena Vista, FL: ESD Association, 1990): 143-150.
9. LG Henry et al., "Transmission Line Pulse Testing of the ESD Protection Structures of ICs-A Failure Analyst's Perspective" in *Proceedings of the 26th ISTFA* (Bellevue, WA: International Symposium for Testing and Failure Analysis, 2000): 203-213.
10. LG Henry, "Differentiating between EOS and ESD Failures for ICs" *Microelectronic Failure Analysis Desk Reference,* 4th ed. (ASM: Materials Park, OH, 1999): 421-436; and in *Proceedings of the 2Oth ISTFA* (Los Angeles, CA: ISTFA, 1994): 117-126.
11. T Polgreen and A Chatterjee, "Improving the ESD Failure Threshold of Silicided nMOS Output Transmission by Ensuring Uni- form Current Flow" in *Proceedings of the EOS/ESD Symposium* 11 (New Orleans, LA: ESD Association, 1989): 167-174.
12. A Amerasekera and C Duvvury,"The Impact of Technology Scaling on ESD Robustness and Protection Circuit Design" in *Proceedings of the EOS/ESD Symposium* 16 (Las Vegas, NV: ESD Association, 1994): 237-245.
13. G Notermans, "On the Use of N Well Resistors for Uniform Triggering of ESD Protection Elements" in *Proceedings of the EOS/ESD Symposium* 19 (Santa Clara, CA: ESD Association, 1997): 222.
14. K Verhaege et al., "Analysis of HBM Testers and Specifications Using a 4th Order Lumped Element Model" in *Proceedings of the EOS/ESD Symposium* 15 (Lake Buena Vista, FL: ESD Association, 1993): 129-137.
15. SG Beebe, "Characterization, Modeling, and Design of ESD protection Circuits" Technical Report No. ICL94-038, (Stanford, CA: Stanford University, 1994).
16. LG Henry, "Comparisons between the ESDA and the JEDEC HBM standards," Disclosures to the ESDA HBM Working Group (WG-5.2) in 1998 and 1999.
17. J Barth et al., "TLP Calibrations, Correlation, Standards and New Techniques," in *Proceedings of the EOS/ESD Symposium* 22 (Anaheim, CA: ESD Association, 2000): 85-96.
18. A Bridgewood and Y Fu, "Comparison of Threshold Damage Processes in Thick Field Oxide Protection Devices following Square Pulse and Human Body Model Injection" in *Proceedings of the EOS/ESD Symposium* 10 (Anaheim, CA: ESD Association, 1988): 129.
19. "Calibrating TLP Systems" Barth Electronics TLP Application Notes (Boulder City, NV: B.E. Inc. [cited 2 March 2001]). These notes can be downloaded from the Web site *http:llwww.* barthelectronics.com.

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