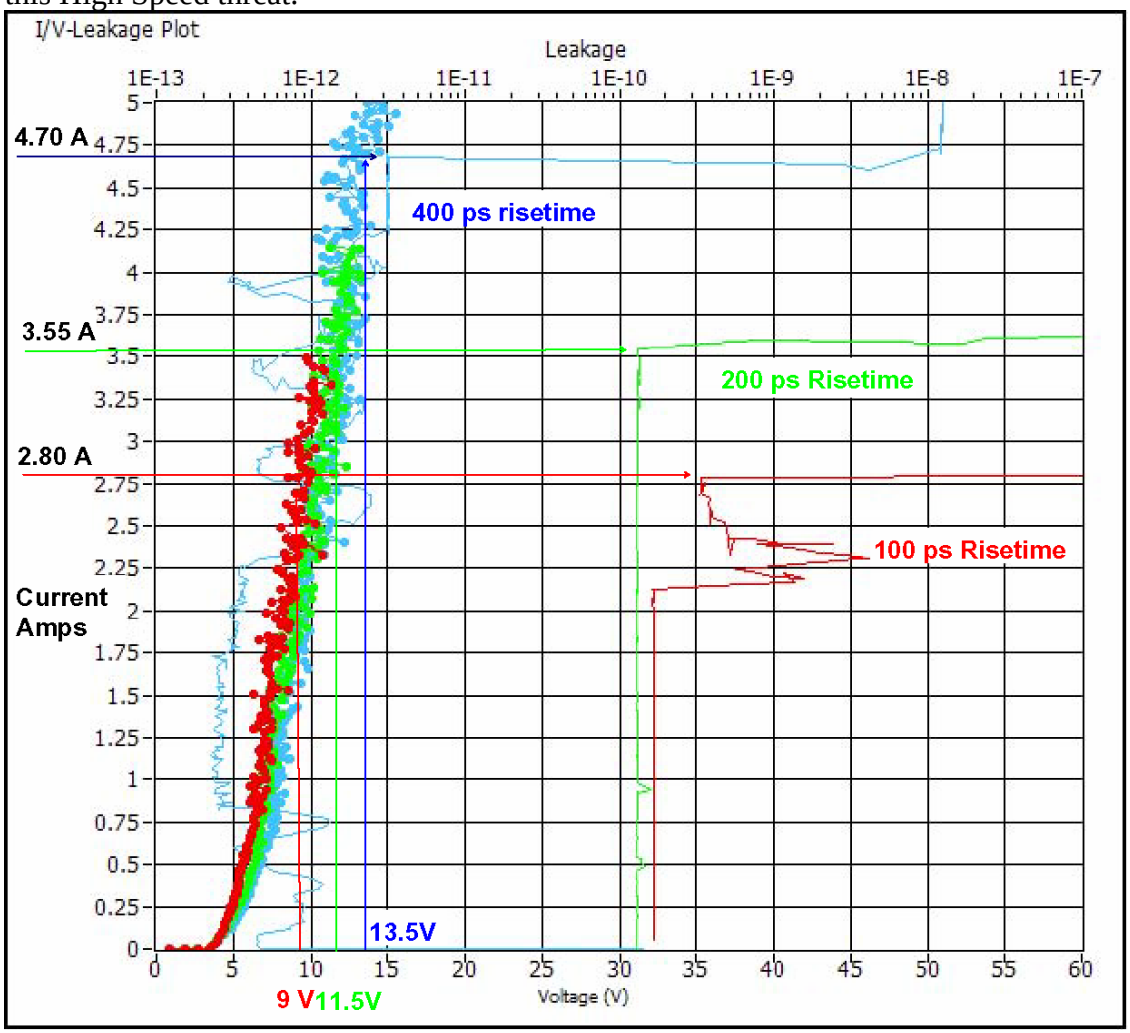
Barth Plots the “Real” CDM Killer of Gate Oxides

Being able to measure and provide the total voltage over time in an ESD test is a significantly new advancement in ESD design. This is especially true for CDM design because voltage kills Gate Oxides. Modern oxides are thinner and have greater sensitivity to over-voltage. The extremely short but very high voltage requires a new test to measure this High Speed threat.



This above plot shows the ordinary I-V plot of a protection circuit which begins conduction at 4 volts and reaches 10 or 15 volts at currents where the gate oxide fails. The ordinary I-V data averaged during the measurement window at late time doesn’t provide the data needed. Current, is not what damages gate oxides however; the short impulse of voltage is the real threat.

Until recently the true parameters of the very fast voltage waveform threat to gate oxides was unavailable. Because CDM can be as fast as 100 ps risetime, this very fast risetime must be available to simulate the real CDM event. Sensors to measure any rate of rise must be at least three (3) times as fast as the risetime being measured. Barth Electronics

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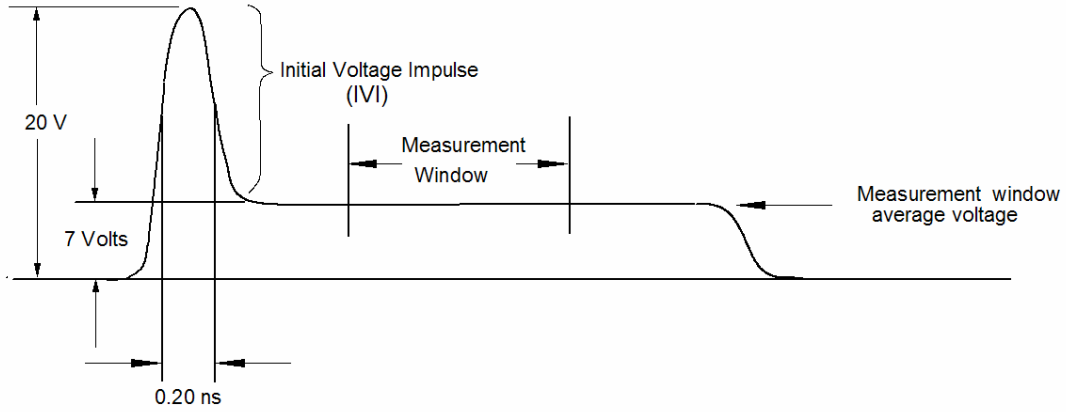
has recently developed sub-nanosecond sensors which allow accurate measurements of both the very fast risetime current and voltage in CDM protection circuits.

Sensors to measure any rate of rise must be at least three (3) times as fast as the risetime being measured. Barth Electronics has recently developed 30 ps risetime capable voltage and current sensors to provide accurate measurements of the very fast risetimes inherent in CDM protection circuits.

We capture all High Speed data in the current and voltage waveform. The very fast voltage which results from that current pulse is the important parameter needed for CDM protection design. Without 30 ps risetime sensor response, the true voltage threat information necessary for CDM design is not available. The Barth Model 4012 now uses 30 ps risetime I & V sensors to provide accurate measurements of 100 ps risetime pulse used to simulate the CDM event threat.

The drawing below shows a typical DUT voltage waveform on wafer which ultimately damages the gate oxide.



Initial Voltage Impulse threat to Gate Oxides
Caused by delay in semiconductor conductivity

The average voltage in the measurement window occurs long after the all important initial impulse voltage. The peak voltage amplitude and its width can now be accurately measured with the High Speed Barth Model 4012 VFTLP+ system. It can measure the sub-nanosecond voltage impulse threat to gate oxides.

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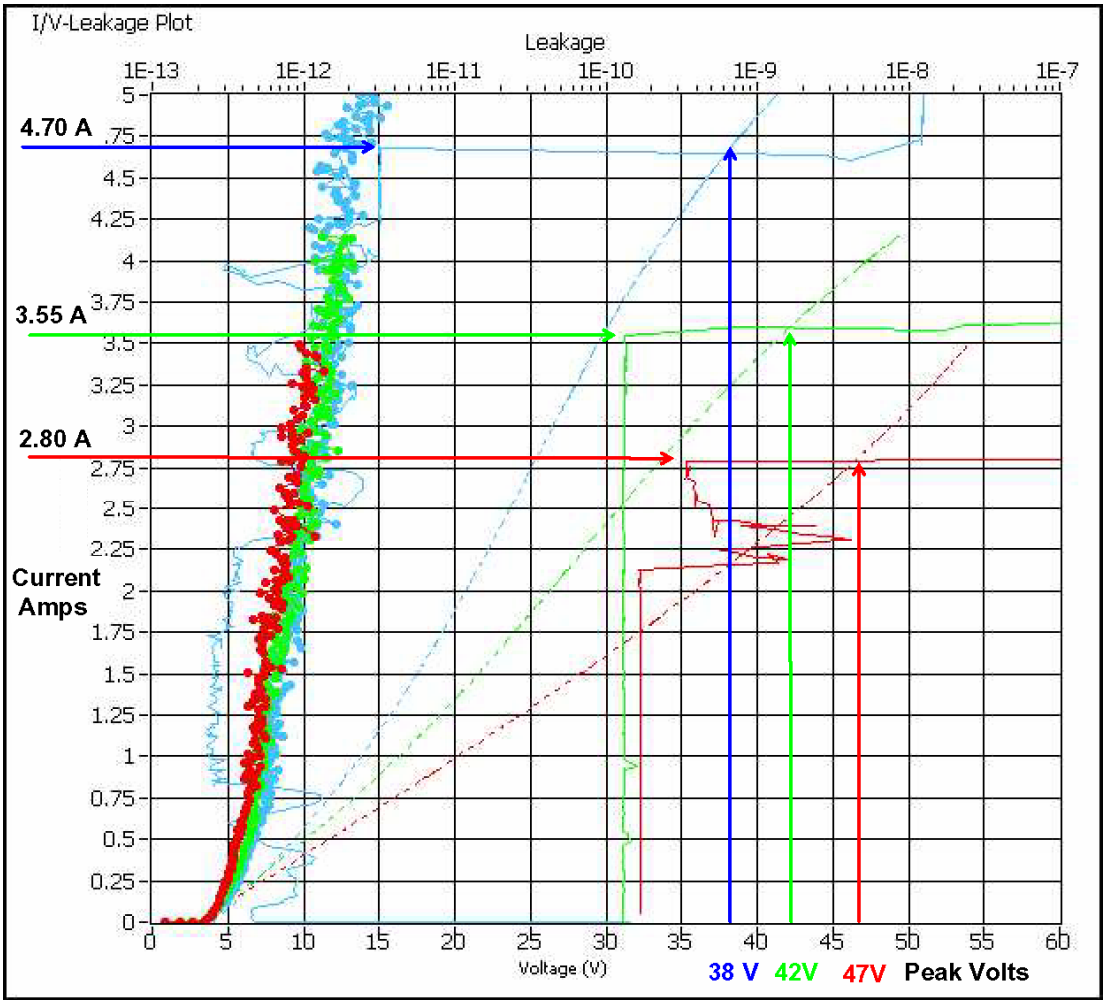

The above I-V plot made with the Barth Model 4012 VFTLP+ shows not only the voltage averaged during the measurement window, it shows the much higher peak voltage that is the primary threat to gate oxides. The much higher initial peak voltage is a much greater threat than the average voltage measured after the semiconductor has fully turned on.

The Barth Model 4012 system is the only VFTLP+ with extremely fast sensors which can measure this extremely short voltage and identify the dangerous sub-nanosecond peak amplitude. From the sub-nanosecond to many nanoseconds, the 4012 system is fast enough to show both the amplitude and width of over-voltage threats to gate oxides. Gate oxides can be killed by voltages too fast and too short to be accurately seen by ordinary VFTLP systems. Can your VFTLP system show the true data that is this fast?

Does your designer have enough time to design CDM with a VFTLP system which isn’t fast enough to show the Real threats? This VFTLP provides the data you need to determine how your CDM protection responds to the real threat. Real analysis for real first time design, the Barth Model 4012 VFTLP+ can do it!!

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