Barth 4012 Application note #1

Revised 03/07/07

CDM Circuit Turn-On Analysis Using Very Fast TLP (VFTLP+) Waveforms

The 4012 Very Fast TLP (VFTLP+) system captures DUT voltage and current waveforms in addition to generating I/V data. The machine was built with the best possible hardware so that software could analyze and extract accurate data from these captured waveforms. This machine has the ability to capture and save waveforms for both the current through the DUT and the voltage across the DUT. The number of I-V waveforms displayed on the waveform screen is determined by the position of two cursors on the I-V plot screen. By moving each of the two cursors the user can display one or many DUT voltage and current waveforms.

The position of the pads for this test chip, required that we use the negative test pulse. Future software will allow the I-V data to be put into the first quadrant and display all waveforms as positive going for ease of visual analysis.

The I-V plot in Figure 1. shows three I-V characteristics of an excellent CDM protection circuit at different pulse widths. We made all three pulse width measurements on one CDM protection structure avoiding failure levels known from previous tests of identical test structures. The green data points are from the 1 ns long test pulse which didn't fail at the maximum test pulse amplitude which produced 18 amps at 17 volts in the DUT. The blue I-V data points from 2 ns pulse testing was terminated at about 12 Amps to avoid failure which occurs at about 16 amps. Because the 5 ns long test pulse was the last test on this structure it was taken to failure, which occurred at about 7 amps. This particular CDM test structure was very robust and provides an excellent demonstration of the capabilities of our 4012 VFTLP+ machine.

These structures had gate monitors to simulate the sensitive gate in the core being protected, and are the failure level indicators when leakage current increases. There is a way to make certain that the greatly increased leakage current was caused by gate monitor failure. If a retest of the test structure produces the same I-V characteristics, this indicates that the protection circuit was unchanged, and undamaged.

Failures current levels of devices at different pulse widths will be more thoroughly analyzed in the future. The ability of the VFTLP+ to provide actual DUT voltage amplitude waveforms into the core will allow more precise analysis of how gate oxide failures compare to Time Dependant Dielectric Breakdown measurements made with flat top pulses.

Measuring the same CDM test structure at three different pulse widths is useful because it shows how the circuit conductivity changes with shorter and longer pulses.

Barth Electronics, Inc.
1589 Foothill Drive, Boulder City, NV 89005
www.barthelectronics.com

Phone 702-293-1576
Fax 702-293-7024
beisales@barthelectronics.com

The 1 ns (blue), 2ns (red), and 5 ns (green) long test pulse I-V data shows how multiple I-V plots are displayed on the same screen.

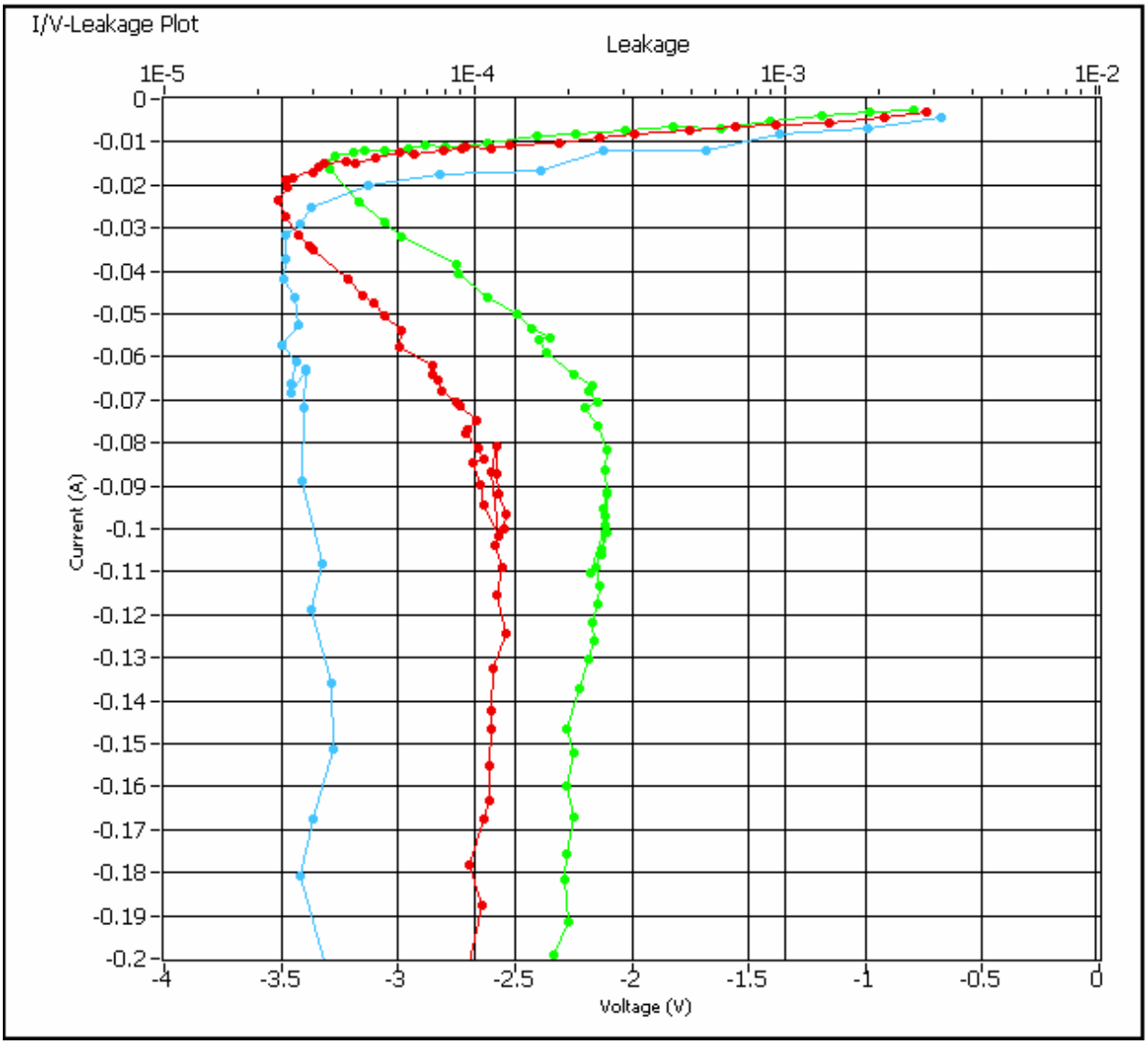


FIG 1

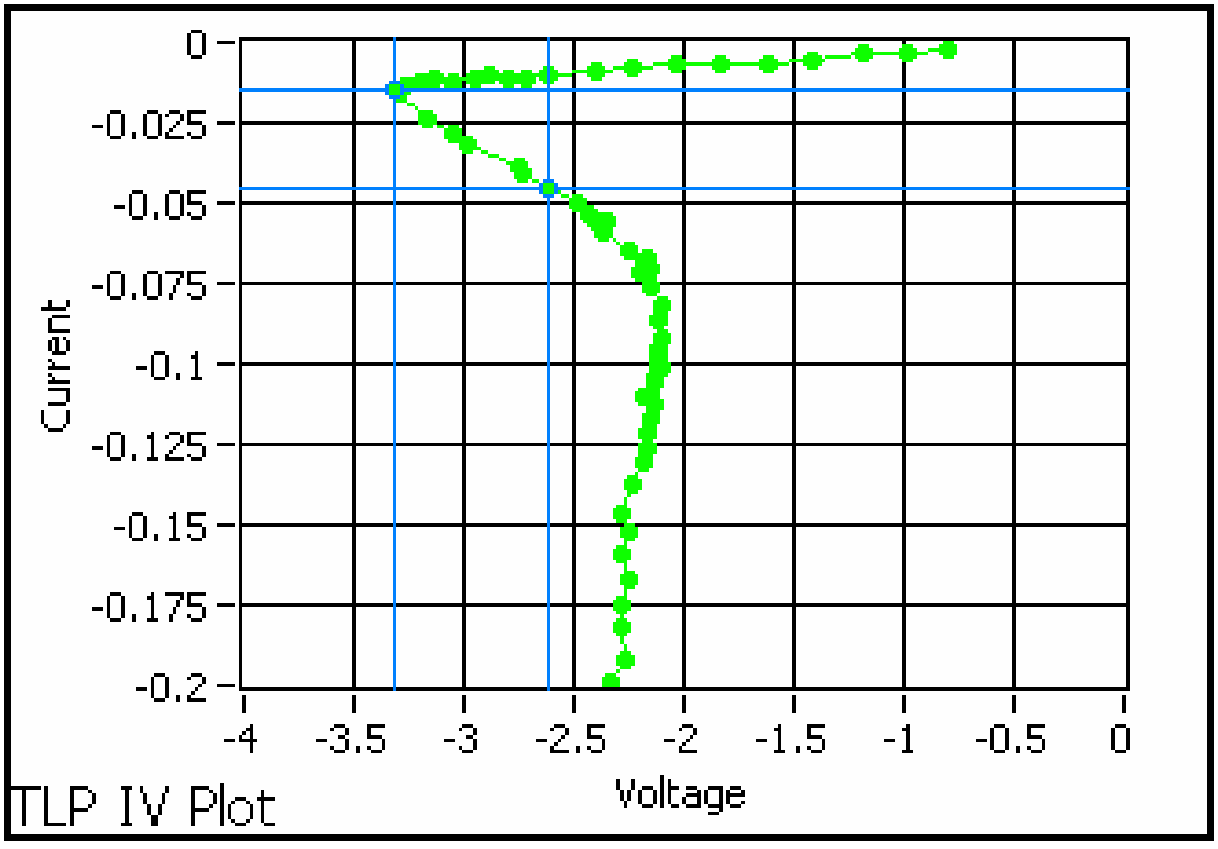
The blue plot shows how the device turns on at 1 ns pulse width. The pulse is so short that the circuit doesn't have sufficient time to fully conduct into its snap-back mode. An approximate measure of the negative resistance at the slight snap-back conditions indicate that it would be about -0.60 ohms. This short pulse test shows that the circuit cannot get into its higher conduction made to cause the voltage decrease to amplitudes it will have when the test pulse is longer; but although the voltage remains higher throughout increasing current pulses, the shorter pulse width does not cause this gate monitor to fail at the maximum test pulse amplitude.

The red plot is made with the 2 ns long test pulse and shows the beginning of the snap-back operation. It shows a noticeable decrease in DUT voltage after snapback. Its snap-back negative resistance can now be measured at about -16.7 ohms.

The green plot is made with the 5 ns long test pulse and shows a more conductive snap-back operation that holds the voltage at even lower levels. The negative resistance during snap-back is now noticeably higher at -23 ohms. Again this test structure is an excellent example of a very well designed test structure that turns-on as desired for CDM protection.

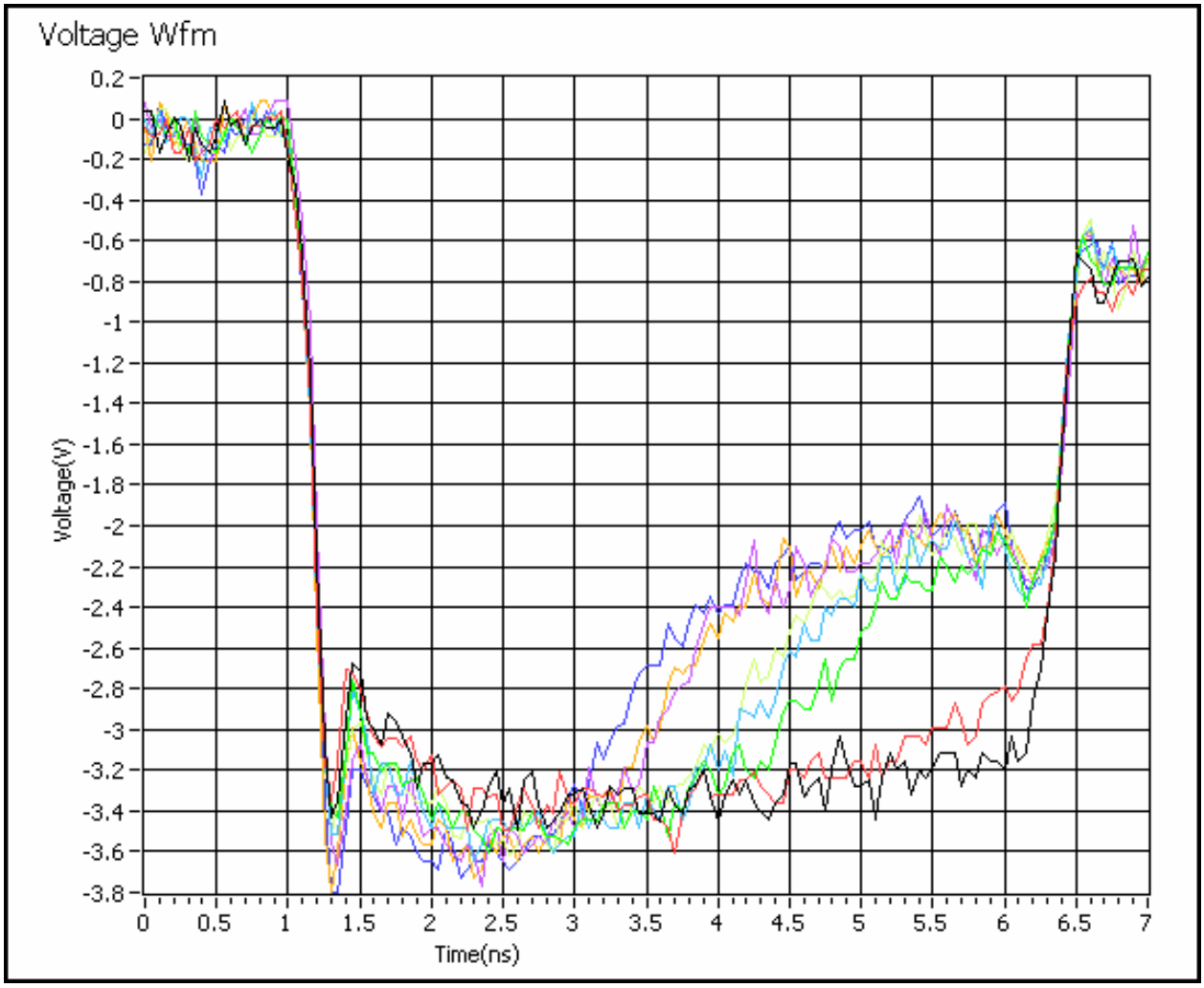
The user can display many different color plots on this screen but keeping them to 8 or 10 plots on one screen limits data confusion when the complete I-V range is displayed. When current and voltage scales are expanded, however, the difference between multiple plots becomes very clear. Subtle differences in multiple similar plots I-V plots can be clearly identified in this way. Although the noise levels in VSTLP increases above a few amps there is a significant advantage in data analysis when using a TLP systems with accurate measurements at all time ranges. Lower accuracy VFTLP systems will provide lower accuracy information on the differences between minor changes in ESD circuit design.

The green data points below form the I-V plot of the 5 ns long test pulse data in the low current region of a CDM circuit where turn-on begins.



The 4012 VFTLP+ software uses two blue cursors used to select two I-V data points which includes all the data points between them. The seven (7) green DUT data points select the all the voltage and current waveforms to be displayed on two more screens for analysis of turn-on characteristics.

The **voltage waveforms** below show a number of interesting facts.



1. The lowest voltage data point is the black trace where it is relatively constant throughout the length of the five (5) nanosecond test pulse.

2. The second higher voltage waveform point is shown as red. It shows a slight decrease in voltage near the end of the 5 ns pulse as the circuit starts to conduct in a nonlinear fashion.

3. The next higher voltage waveform is shown in green. It also shows a significant decrease over the last nanosecond of the 5 ns long pulse.

4. The highest current point between the two green cursors on the I-V plot is shown in blue on both the DUT Voltage and Current plots. Here the voltage has started to decrease after about 3 ns and shows major voltage decrease during the last 1.5 ns of the 5 ns long test pulse. The current increase after a few nanoseconds occurs at the same time as the decreasing voltage.

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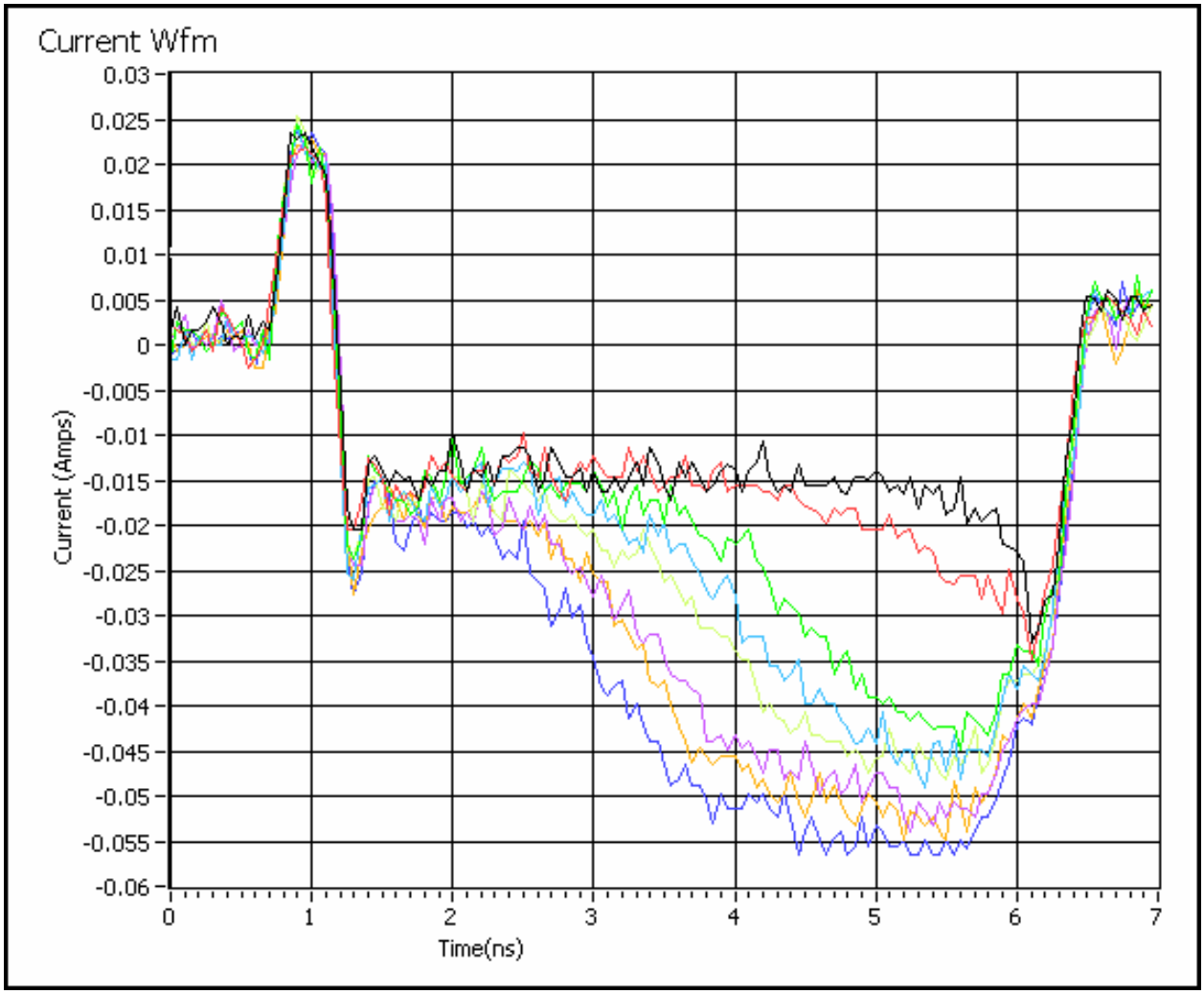
beisales@barthelectronics.com

The **current waveforms** between the two selection cursors are shown below.



1. Again the lowest test pulse amplitude is the black trace which is relatively constant throughout the length of the five (5) nanosecond test pulse.

2. The second higher current waveform is shown in red. It shows a slight increase in current near the end of the 5 ns pulse as the circuit starts to conduct in a nonlinear fashion.

3. The next higher current waveform is shown in green. It also shows a significant, linear increase over the last nanosecond of the 5 ns long pulse.

4. The highest current point between the two green cursors on the I-V plot is shown in blue on this DUT Current waveform. Here the current has started to increase after just 1 ns and shows a major linear current increase during the middle ns of the 5 ns long test pulse. The current increase after a few nanoseconds occurs at the same time as the decreasing voltage.

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These are just seven waveforms for this particular CDM protection circuit during its interesting turn-on phase. The waveforms at all the higher currents with voltage and current amplitudes during the pulse are also available. Many more details beyond this cursory analysis will certainly be extracted from accurate waveforms, when studied by ESD designers.

One of our associates in ESD design commented that a Very Fast TLP (VFTLP+) system would not show any useful CDM design information. He must have forgotten the limited understanding of early TLP data, with the limited accuracy available from early crude machines. Today TLP data has such extreme value that all ESD design tutorials make specific demands that is must be used if efficient and good ESD protection is to be achieved.

Barth Electronics has complete confidence that intelligent ESD designers will devise methods to extract, and expand on the preliminary analysis of VFTLP+ waveforms made here. That is why we have invested so much time in developing the most accurate fast pulse hardware and waveform capture software for sub nanosecond time analysis of CDM protection circuits. Improvements in protection circuit design can grow rapidly when accurate sub-nanosecond voltage and current waveforms details are used.

An analysis of all the waveforms, at increasing amplitudes can now identify how the CDM protection circuit turns on during the test pulse time. Knowing the dynamic conductivity at each period of time can now provide the CDM designer with details impossible to measure previously. The data shown here was taken at 100 ps risetime. What additional design data may be able to be extracted from VFTLP+ data taken at slower risetimes of 200 and 400 ps?

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