Introduction to VFTLP+

VFTLP was originally developed to provide I-V characteristics of CDM protection and its analysis has been similar to that of TLP data used to analyze HBM protection circuits. VFTLP and TLP data are an average of the voltage and current waveforms taken in the measurement window. TLP for HBM circuit analysis provides very reasonable average voltage and current data after their waveforms have settled down and are relatively constant.

HBM failures are primarily the result of energy dissipation in silicon protection elements. CDM threats are 1 to 2 ns long, while HBM treats are about 100 to 200 ns long. CDM is different from HBM in two important respects. First, CDM currents create voltages which are applied to gate oxides. Oxides fail when their voltage capability is exceeded.

The second major difference is that HBM testing specifies 2 to 10 ns current risetimes while the CDM event is extremely fast. Its risetime is as fast as 100 ps and the length of its pulses are much shorter. In order for VFTLP to simulate CDM events its test pulse risetimes be as fast as this 100 ps. The original VFTLP test system used shorter pulses with the intention of simulating CDM. However this test still uses the I-V data averaged in the measurement window. Although averaged data is useful in understanding the basic I-V characteristics of the CDM protection element, it misses time varying information. The high speed CDM event creates rapidly changing current and voltages in the silicon protection elements or circuits. Understanding their high speed response introduces a new and very important indicator of CDM protection circuit operation, that is impossible to identify using only current and voltage data averaged during a measurement window.

Because the primary cause of failure with CDM is gate oxide failure, voltage is the primary information needed to understand protection elements or circuits. The high speed CDM event creates very fast rates of current and voltage rise inside high speed IC's. We have developed special 30 ps risetime voltage and current sensors to identify the total DUT response with our VFTLP system. Measuring the high speed operation of silicon elements or circuits on wafer provides a new insight into previously un-known details of protection element operation.

Our VFTLP also adds true 100 ps risetime test pulse capability to simulate the CDM testing and CDM events. To deliver the high speed test pulse to the DUT, we always use very low loss transmission lines. Our very high speed wafer probes achieve extremely low inductance connections to the wafer. We identify this carefully engineered CDM circuit analysis tool as VFTLP+.

Our measurements of protection circuits on wafer have identified oxide threat Time Dependent Dielectric Breakdown (TDDB) voltages. Until now this measurement has been made with rectangular pulses to identify oxide voltage sensitivities to relatively short pulses. We have found that the first part of the oxide voltage threat is the initial voltage impulse. We identify this as the Initial Voltage Impulse (IVI) because it

occurs in every VFTLP+ and CDM event. It is caused when extremely fast CDM events create very narrow voltage impulses, typically being 150 to 200 picoseconds wide. More complex protection circuits take additional time to turn-on and the IVI fall time can be as long as 5 ns. The IVI precedes the average steady state voltage identified in the measurement window. The IVI voltage has been referred to in previous papers although the true peak voltage has not been available. With both limited risetime test pulses and limited DUT response risetime measurement systems, the real silicon IVI cannot be determined. The total oxide threat can now be identified by measurements of the voltage created by silicon protection circuits during the total time the threat is applied.

Diodes are a common element used for CDM protection. To demonstrate how voltage developed across a protection element varies during the test, we measured some micro-miniature silicon signal diodes. These diodes are only one mm long and have very low package inductance. The inductance is low enough that it does not become noticeable until the VFTLP+ current increases to a level high enough to increase the L/R effect. At this time the voltage impulse from –L·di/dt effects become visible. We identify this as the Secondary Voltage Impulse (SVI) because the negative polarity inductive voltage "kick" from fast risetime current flowing though an inductance occurs when chips are packaged.

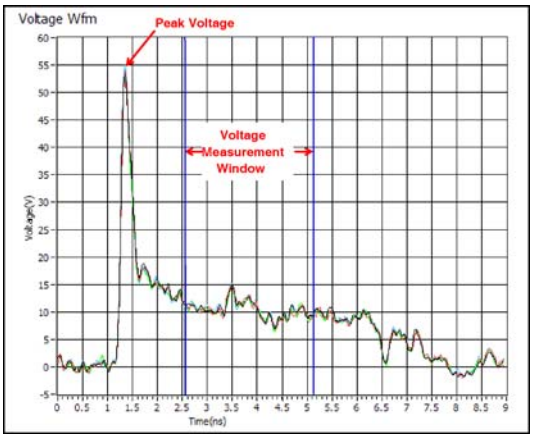

Figure 1. Voltage waveform showing voltage averaged over the measurement window and peak value

Semiconductors have an inherent delay between the time a voltage is applied and the current flow completes the silicon path. Our VFTLP+ system has permitted us to investigate high speed physics of semiconductors. The time delay between the application of voltage and carriers completing their path through silicon is typically identified as being 10 to 20 picoseconds. This time delay is dependent on the path length through the semiconductor and the applied voltage. Higher voltages increase the speed of carriers in semiconductors until the saturation velocity limit is reached.

These introductory measurements of commercial diodes were made on 1N4148 diodes soldered directly to the end of a time calibrated piece of 0.085 inch diameter semi-rigid coaxial cable. The cable is connected to the VFTLP+ tester with an integral SMA connector. Great care must be made to assure that the measurement reference location is positioned at the end of the coaxial test cable where the DUT is located. These measurements can be made with any VFTLP machine on similar diodes. Accurate information on the voltage

overshoot which occurs before the current carriers complete the circuit path through the silicon must be made with 100 ps risetime. Simulating the CDM event is of paramount importance if VFTLP is to provide its inherent capability.

Diode Turn-on Time Measurements

Note: The first measurements made of the 1N4148 miniature size package were made at the end of the two wires, which extend about 0.095 inch past the end of the 0.085" dia. copper jacket.

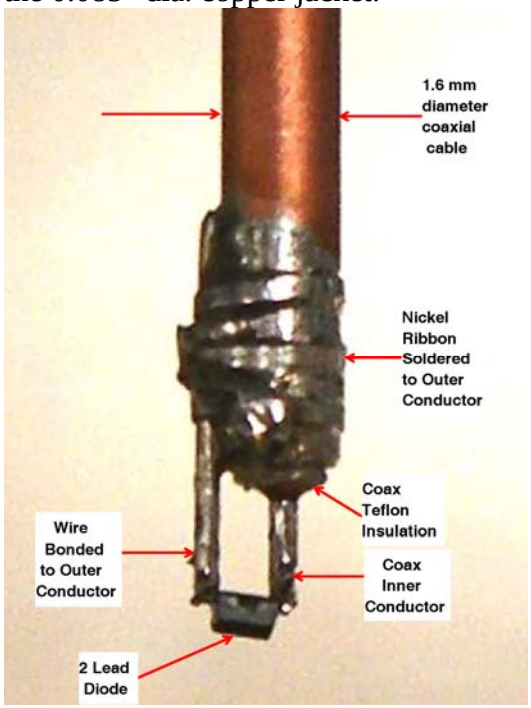

Figure 2. 1N4148 diode mounted on coax

We also made tests of the inductance of these two wires by placing a 0.040 wire short between them 0.070" from the body to simulate the 1N4148 diode position. These relatively short wires extending out from the coaxial cable added a significant amount of inductance.

To remove as much lead inductance as possible we connected the much shorter leads in micro-miniature 1N4448 diodes directly at the end of the Teflon. It was placed between the 50 ohm inner conductor and its Copper jacket. Removing the wire leads and moving the diode 0.095 inch closer to the timing short reference end of the coaxial cable shows noticeably less inductance.

This second diode has the shortest total package lead length and therefore has much less inductance. It is a Digi-key part number MMBD4448HTADICT-ND. The manufacturer's part number is MMBD4448HTA-7. It is in a SOT-523, 3 lead package but only one of the two diodes in the package are used. It is rated at 80V; and 150 mW. Measurements of this small diode positioned directly at the zero time location of the DUT coaxial cable, minimizes the parasitic lead inductance. When measuring packaged parts, the leads out side the package can be made short, but the lead frame and bond-wires to the chip add measurable inductance. The total inductance creates a significant -L·di/dt voltage impulse at the beginning and end of the test pulse. This voltage impulse is added to the Initial Voltage Impulse (IVI) of the semiconductor makes the exact time delay difficult to establish.

These first examples are used to emphasizes the rate of silicon conductivity increase possible to measure with fast rising test pulses on commercial diodes. The voltage IVI and the rate of current increase are similar to some CDM protection circuits which use SCR elements.

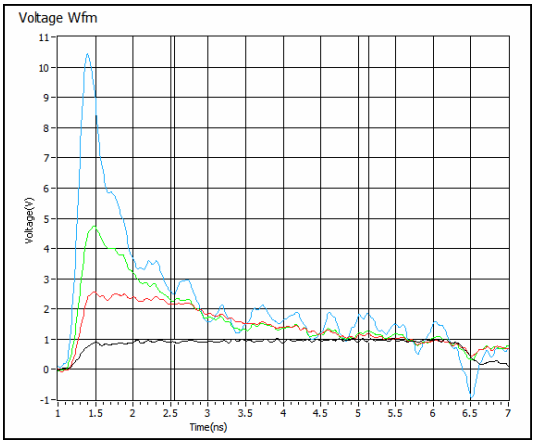

Figure 3. Voltage waveforms of 1N4448 diode from 0 to 0.27 Amps

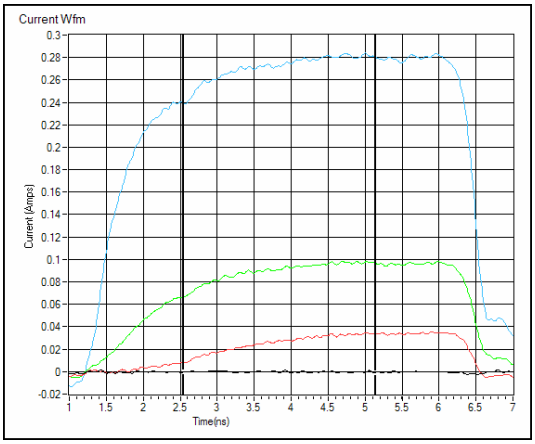

Figure 4. Current waveforms of 1N4448 diode from 0 to 0.27 amps

The first voltage waveform in Figure 3 (black trace) is at about 1 volt and draws no current for the same trace in Figure 4. The voltage is constant at 1 volt. The second test pulse is about 2.5 volts (red) and remains at that level for about 1.5 ns; then begins to decrease to the 1 volt constant silicon conductivity level in 3 or 4 nanoseconds. The 100 ps risetime test pulse creates the high amplitude voltage across the diode. The peak voltage created when using slower risetime test pulses of 200 and 400 picoseconds create lower peak voltages. These large diodes provide excellent examples of the slowly increase in silicon conductivity. After they reach the peak voltage they begin an immediate but slow decrease toward 1 volt over a similar 3 to 4 nanoseconds time period.

There is no current created when the 1 volt test pulse is applied to the diode, as shown in the black trace. The slow increase in current is obvious in the next test pulse (red) as the current requires almost 4 nanoseconds to reach its constant amplitude.

At higher pulse currents the dynamic resistance of the diode becomes lower and increases the –L·di/dt IVI effect. This is shown for higher amplitude pulses as the pulse voltage increases, creating higher currents (green, and then blue). Higher test pulse voltages cause the carriers to move more rapidly and the steady state current is reached more rapidly until carrier velocity reaches saturation.

By replacing the diode package with a conductor having the same dimensions as the diode package leads, the –L·di/dt voltage impulses at the beginning and end of the test pulse can be identified. This is only approximate however, because the physical dimensions of the bond wire from the lead frame to the chip inside the package are only estimated.

Measurement Window Location?

The plot below in Figure 5 would normally indicate a snapback element. However the diode we are testing does not exhibit a snapback characteristic.

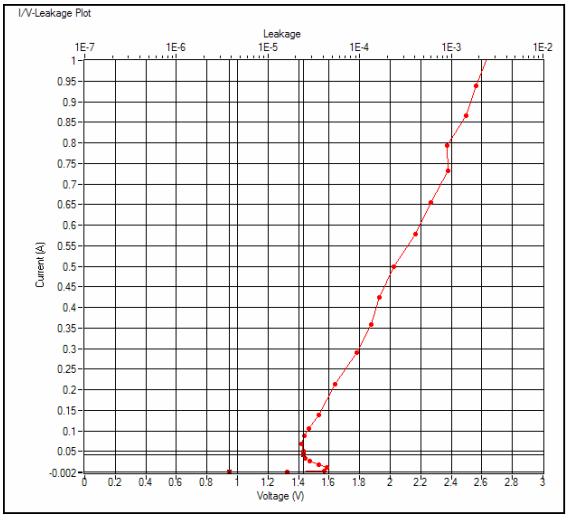

Figure 5. Snap-back suggested by this I-V plot of an ordinary diode.

By examining the voltage waveforms below in Figure 6, we can see that the Initial Voltage Impulse is immediately followed by decreasing voltage. The measurement window indicated by the heavy black lines at 2.5 ns and 5.1 ns shows the average (Vt1) of the decaying voltage being less than the peak voltage of about 2 volts.

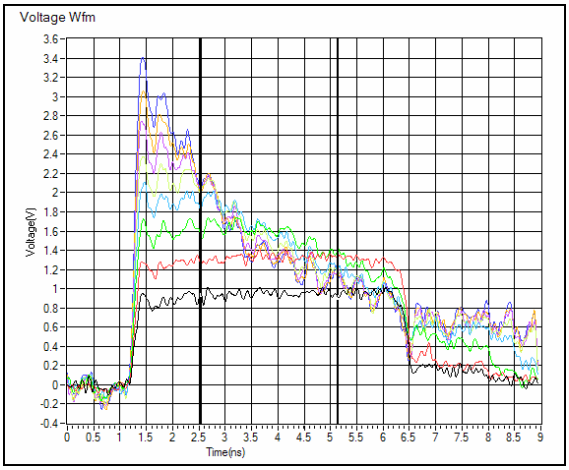

Figure 6. Voltage waveforms measured over 0 to 1 amp range. For clarity only every third waveform is shown.

The waveforms show that the voltage is not a snap-back condition. Because the average voltage in the measurement window is temporarily lower than the average of earlier test pulse voltages, an average measurement gives a false indication of snap-back.

Measurements of the 1N4448 diode were made with a 5 ns long pulse. As shown in figure 6, the first three test pulses produce very low current and immediately fall to zero at the end of the pulse.

At higher amplitude test pulses the voltage and current are seen to continue after the end of the 5 ns long test pulse. This is the stored charge effect in the diode. Depending on the silicon protection element characteristics, this voltage sometimes continues at a significant amplitude. This can add voltage for some part of a nanosecond to the TDDB threat. If the length of time a voltage is unexpectedly extended across a gate oxide, during either VFTLP or CDM test pulses, GOX failures can be lower than expected.

To display both the average and peak voltage we introduce the dual voltage plot shown below in Figure 7. It displays the total voltage threat very clearly by adding the peak voltage to the usual VFTLP I-V average current and voltage plot shown in Figure 5 above.

The total voltage threat in a single display provides a simple but effective graphical presentation. The ordinary I-V data in this plot is the same as that shown in Figure 5.

By adding the peak voltage to the I-V plot, both threats produced by CDM protection circuits can be rapidly analyzed.

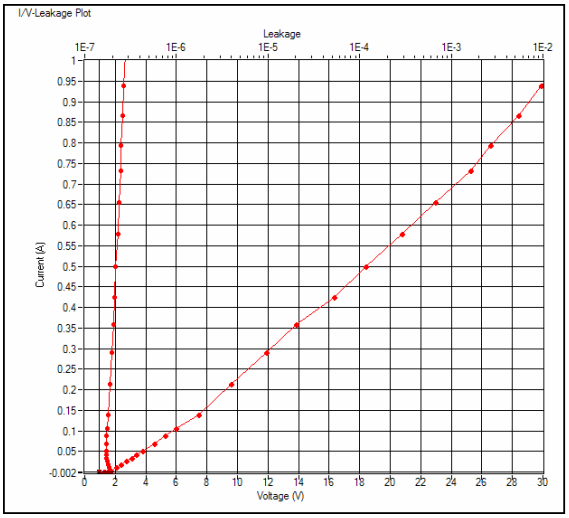

Figure 7. I-VV plot from 0 to 1 amp adds the peak voltage measurements to the standard VFTLP Plot .

We identify this as an I-VV plot because both the average and peak voltage are measured and graphically displayed.

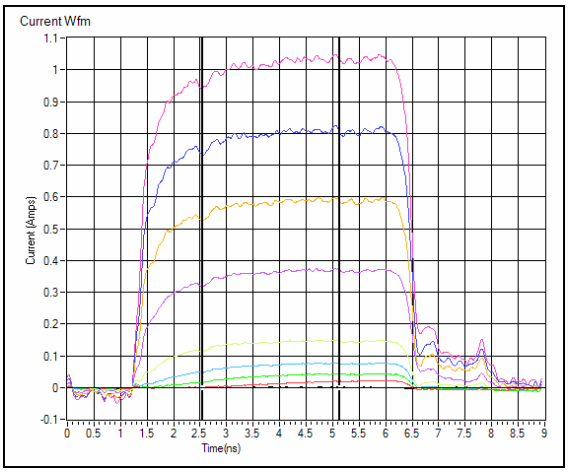

Figure 8. Current waveforms from 0-1A

This figure shows the current waveforms increasing more rapidly as the test pulse amplitude increases. Increasing test pulse voltages increase the speed of the carriers through the silicon element. The large path length in the individual diodes tested here creates a longer path than is found in ESD protection elements. Therefore the IVI in simple ESD diodes is much lower, however more complex ESD protection elements such as an SCR can have very similar rates of voltage decay with very high peak voltages.

Conclusions

The ability to simulate CDM rates of rise and measure its effect on silicon protection circuits is provided in the VFTLP+ test. While we measured diodes larger than those used in ESD protection, it demonstrates the high speed measurement capabilities needed to understand the high speed operation of silicon. Commercial diodes such as the ones we tested do not fail at the highest pulse current and longest pulses. They are readily available and their time delay characteristics are very repeatable.

The waveform and I-VV plot data provided by this VFTLP+ test adds completely new analysis to the original VFTLP system. Improving CDM protection is important because the sensitivity of gate oxides continues to increase.

We are eagerly searching to test CDM protection on wafers. This new analysis tool can provide an important data base for ESD design. This information will be the first time manufacturers of wafers will be able to see the complete protection element characteristics at the high speeds which simulate the CDM test.

The wafer information we measure and publish will be isolated from other manufacturers, because this type data has never been published previously. We need to measure more silicon elements or circuits on wafer to assemble VFTLP+ information as an introduction for the industry.

This data is the first of our application notes for this VFTLP+ test system. Those who supply wafers for this testing will be the first to receive full information time history on their CDM protection design details and the effects geometry variations have on gate oxide failures.

We will continue to publish application notes to develop a better understanding of circuit response to high speed threats. This test method can begin a correlation between voltage response and variations in geometry. Voltage and current waveforms on future silicon CDM protection will become more analytical as dimensional details are better understood.

We can provide this information to begin a better understanding of previously hidden operational parameters of high speed ESD protection.

This first presentation demonstrates how ordinary VFTLP has been improved to expand design data it is now possible to extract from CDM protection elements. We have devoted over two years to this test system and will continue to expand the value of this new analysis tool.

Our measurements of actual CDM protection circuits and individual test structures data will continue in future application notes. The generosity of potential customers, in providing silicon protection elements on wafer has been most helpful in understanding the basics of high speed silicon protection. The small amount of data we have recently measured provided the basic requirements needed for CDM design. This new source of data begins a new ability to analyze the high speed operation of silicon elements and circuits in continuous time detail.

Jon Barth
Chief Engineer

Barth Electronics Inc.
e-mail jonbarth@ieee.org
1589 Foothill Dr.
Phone (702) 293-1576
Boulder City NV 89005
Fax (702) 293-7024