The SDM Test Method: Past, Present, and Future

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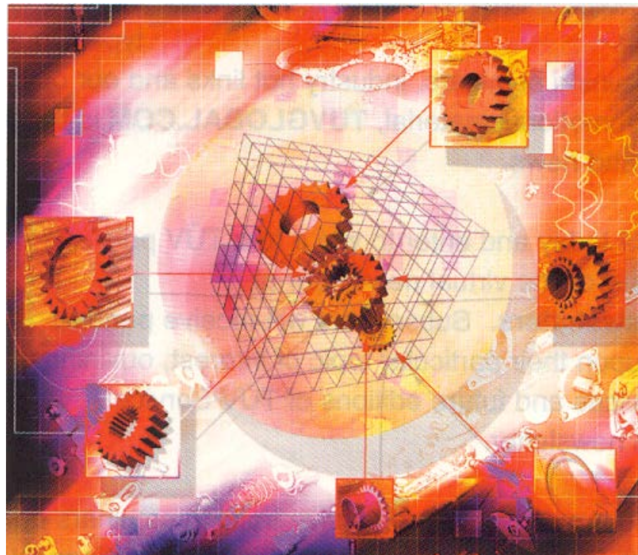
***The socketed-device model has been a work in progress since the early 1990s*.**

Evaluating the sensitivity of electronic components to electrostatic discharge (ESD) is a key element in controlling and preventing ESD damage. The test procedures used to characterize, determine, and classify the ESD sensitivity of components are based on three basic models of ESD events: the human-body model (HEM), machine model (MM), and charged-device model (CDM). These models differ in that HEM and MM simulate the electrostatic transfer of a charge to a device, whereas CDM simulates the electrostatic transfer of a charge from a device. This article will focus on the charged-device model and examine issues surrounding a specialized CDM test method based on the socketed-device model (SDM).

Since the early 1990s, the ESD Association (ESDA) Device Testing Working Group 5.3 has labored to draft a socketed-charged-device model (S-CDM) test standard. In the S-CDM test method, the device under test (DUT) is placed in a socket, and, in theory, only the capacitances of the DUT and socket are charged. However, attempts to build a test system capable of charging only the DUT and socket have been unsuccessful: Elements of the entire test system are unintentionally charged and affect the discharge event. Consequently, the Device Testing Group now defines this type of CDM test method as the SDM test method.



To better understand the differences between S-CDM and SDM tester-simulators, we will review the history of this complex test method, the current design of existing ESD test equipment, how charge is stored differently in SDM versus robotic CDM (R-CDM) test systems, and how this difference can produce a divergence in test results. Finally, we challenge ESD test-equipment manufacturers to build a second-generation S-CDM test system.

SDM History

SDM terminology was developed in 1997 by Working Group 5.3.2. The term was derived from S-CDM testing, which refers to the CDM testing of an integrated circuit (IC) mounted in a socket. This contrasts with R-CDM, or nonsocketed CDM (ns-CDM), testing, in which the IC is tested in a dead-bug (pins facing up) configuration and the plastic package is in intimate contact with a charge plate during the charging process.[1] Figures 1 and 2 illustrate the two types of CDM test equipment.

These test methods are intended to simulate discharge events that occur when a charged IC discharges directly through one of its pins into a very-low-impedance ground, because real-world CDM events can occur during automatic handling or placement of ICs during manufacturing operations.[2] The discharge-current waveforms from the test equipment show very fast rise times (<1 nanosecond) and very short pulse duration (<20 nanoseconds; see Figure 3).

Both test methods can produce failure mechanisms such as gate oxide ruptures in the ICs.

The first CDM tester-simulator was designed in 1979.[3] Tester design improvements attempting to reproduce real-world air-discharge CDM events (R-CDM) were made during the late 1980s and early 1990s.[4,5] Although these simulators proved valuable for reproducing field failures, they proved only marginally successful for devices with very small pin pitches and high pin counts. Consequently, test-equipment manufacturers were asked to produce an automatic simulator that would increase the IC manufacturer's throughput; hence, the S-CDM tester-simulator was born.

Although S-CDM and R-CDM test equipment were

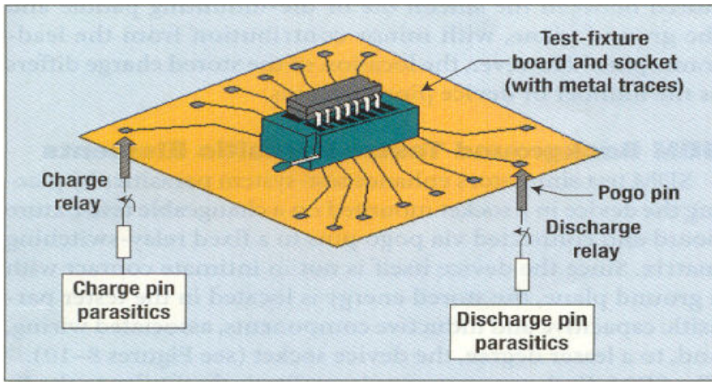


Figure 1. Socketed CDM

designed differently, both produced gate oxide failures in many ICs. Early versions of the ESDA CDM standard, CDM WIP5.3, included both methods.6 Separate specifications for peak current, rise time, and pulse duration values were given for each type of CDM test method due to the significant waveform differences (see Figure 3). From 1992 to 1996, Working Group 5.3 believed that both test methods could exist in a combined CDM test standard.

However, as more IC manufacturers began using both types of CDM test equipment, major differences in test results occurred. When ICs with different package configurations-and therefore, variable package-capacitance values-were tested, the S-CDM test system results did not produce failure voltages comparable to R-CDM levels.7-10 For example, S-CDM failure voltages remained constant regardless of package configuration and capacitance, whereas the R-CDM simulator produced failure voltages that varied as a function of the package capacitance. In other words, the S-CDM test system could not distinguish between ICs with different package-capacitance values.[8-11]

Failure analysis of ICs tested using both R-CDM and S- CDM simulators frequently showed the same failure site, but the ICs tested using S-CDM exhibited more-severe gate oxide damage (see Figures 4 and 5).[12-14] In some IC technologies, the S-CDM simulator produced electrical failure signatures that could not be reproduced by the R-CDM test system. [14] Attempts to find a general failure-voltage correlation between the test simulators were unsuccessful, although a very limited one was achieved for some complementary metal-oxide semiconductor {CMOS) technologies.[12]

In 1996, Working Group 5.3 split the R-CDM and S-CDM test procedures into separate documents due to inconsistent failure results and no failure voltage correlation between test simulators. The same committee decided in 1997 to rename the S-CDM test method to the SDM test method and create the new SDM Working Group 5.3.2. A detailed analysis of the operation of the Group 5.3.2. A detailed analysis of the operation of the commercially available SDM tester was published in 1998.[15] The paper discussed how the test simulator operated and why a separate SDM standard test method could not be written. In 2000,5.3.2 published a technical application report explaining the SDM test system's unique capabilities and limitations, as well as how it could be used to perform CDM testing.[16]

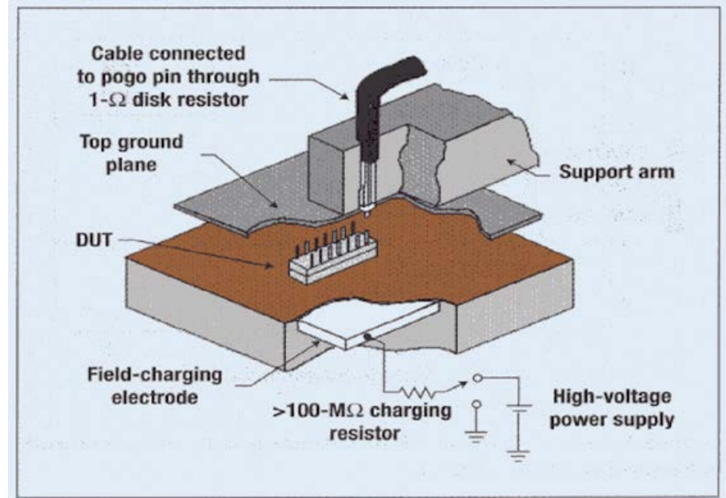


Figure 2. Nonsocketed CDM

First-Generation SDM Test System

A simplified block diagram of the major components with- in existing SDM test systems is shown in Figure 6. The basic elements consist of a high-voltage (HV) power supply, computer-controlled relay-switch matrix, test-fixture board and sockets, HV relays, and computer-controlled ground-switch relays. This design enables the user to place an IC into a socket on the test-fixture board, define the pins to be charged and discharged, set a charging-voltage level, and automatically run the test. In addition, test systems typically include parametric curve trace and leakage measurement equipment, which can be used to check for pin electrical characteristics before and after stress. The parametric curve trace measurement, which can only partially detect electrical failure signatures, has proven very useful for screening weak or extremely sensitive pins.[16]

Differences in Device and Tester Capacitances

In SDM testers, a significant amount of parasitic capacitance and inductance is added to the DUT (see Figures 7-10).[14] When a packaged IC is placed into a socket and the stress volt- age is raised to a specific value, the IC, socket, and background tester parasitics are all raised to the same potential. After the HV relay switch connects a specified pin to ground, the total charge in the system is discharged. This total charge represents the charge stored in the IC, as well as the socket, test- fixture board, parasitic capacitors in the HV charge line, and unused floating pins in the socket or test-fixture-board assembly. Generally, the total background charge can be much more than the charge stored in the IC and its package. [15]

In contrast, device capacitance for R-CDM test simulators is generally defined as the capacitance formed by an IC in relation to a ground plane (see Figure 7). With the device in a dead-bug configuration (see Figure 2), the capacitance contributions can be summarized as follows: First, the field- charging electrode of the tester represents one electrode of the device capacitor. Second, the package material and the dielectric on the field-charging electrode represent the dielectric of the device capacitor. Finally, the lead frame and silicon die much less than

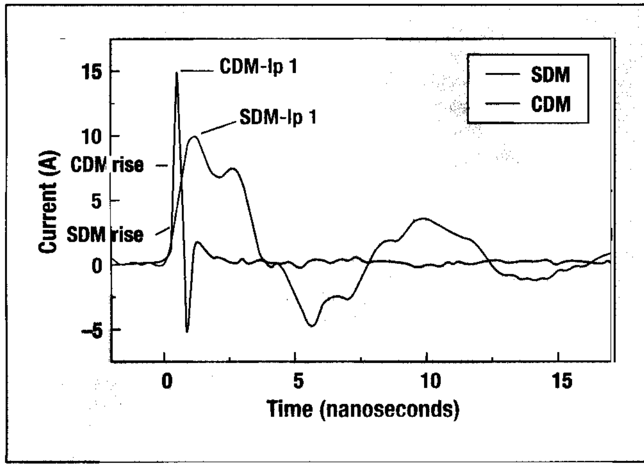


Figure 3. Typical CDM and SDM discharge-current Waveforms (charging voltage: 1000V)

represent the second electrode of the device capacitor. Prior to discharge, the first electrode (the field -charging electrode) will be at ground, and the second electrode (the lead frame and silicon die) will be at a charging potential (i.e., 1 kV). Note that within the IC there is no voltage difference after charge-up and before discharge.

In the R-CDM method, the charge is stored mainly in the IC package (between the lead frame and the external ground plane), and not in the parasitic elements of the simulator. In small plastic-packaged devices, the majority of the charge is stored between the silicon die or die-mounting paddle and the ground plane, with minor contribution from the lead-frame pins.[5] However, the location of the stored charge differs as the number of device pins increases.

SDM Background Tester Parasitic Elements

SDM test simulators enhance test-systern parasitics by placing the device in a socket mounted on a changeable test-fixture board and connected via pogo pins to a fixed relay-switching matrix. Since the device itself is not in intimate contact with a ground plane, the stored energy is located in the tester parasitic capacitive and inductive components, associated wiring, and, to a lesser degree, the device socket (see Figures 8-10).[15]

The SDM discharge sequence is qualitatively similar to the R-CDM sequence (e.g., discharge pin, device, and capacitance on other nongrounded pins) but is quite different in quantitative terms. For SDM, the IC package capacitive components are relatively small, whereas the parasitic capacitance on the pins due to the tester can be quite large. In fact, it can be so large that failures can occur to a pin not used as a direct-discharge pin.[15]

Figure 11 shows a simplified schematic of the background tester impedance at each socket pin of a typical SDM test system. The changeover relay normally connects to four reed relays. Hence, the capacitance (C) associated with these four relays is connected to the socket pin via a copper trace on the test- fixture board between the device socket and the relay ma - trix. Each device pin electrically inserted into the socket sees this same parasitic background capacitance. When energized,

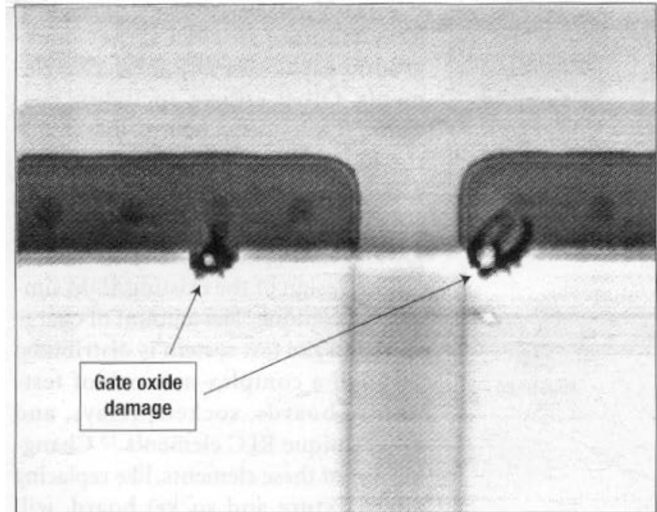


Figure 4. R-CDM gate oxide damage.

the changeover relay is connected to ground and provides a discharge path for the SDM event.

Although one pin is designated as the charge pin, capacitive coupling charges all adjacent pins on the HV-relay board when the pin under test is charged. After the charge-up sequence of the SDM test, all pins on the board reach an equal voltage. Hence, the total charge in the test system includes the charge stored in the device and all of the charge associated with the other internal tester RLC parasitic elements (see Figures 8-10). Because there is significant background tester capacitance of all device pins in the tester (20-30 pF), a change in the pack- age configuration design (e.g., from PLCC28 to PQFP44) may be insignificant to the total capacitance of the test system.[9] For example, a small change in device capacitance, from 2.8 to 4.4

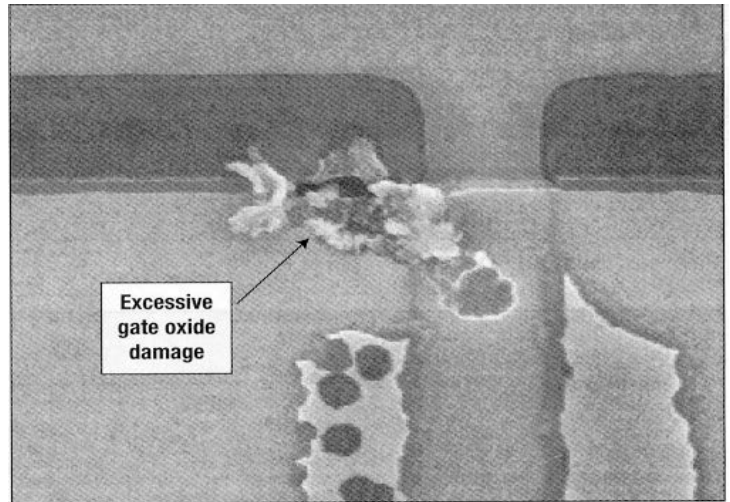


Figure 5. S-CDM poly melt and gate oxide damage.

pF, represents an increase of 157% for the device in the R-CDM test system; however, the same change represents 5% of the distributed capacitance in the SDM test system.

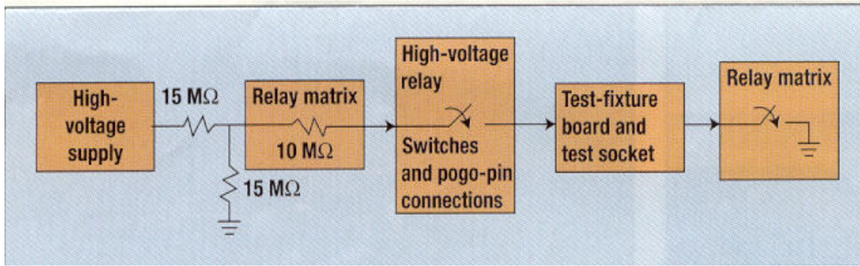


Figure 6. Existing SDM test systems.

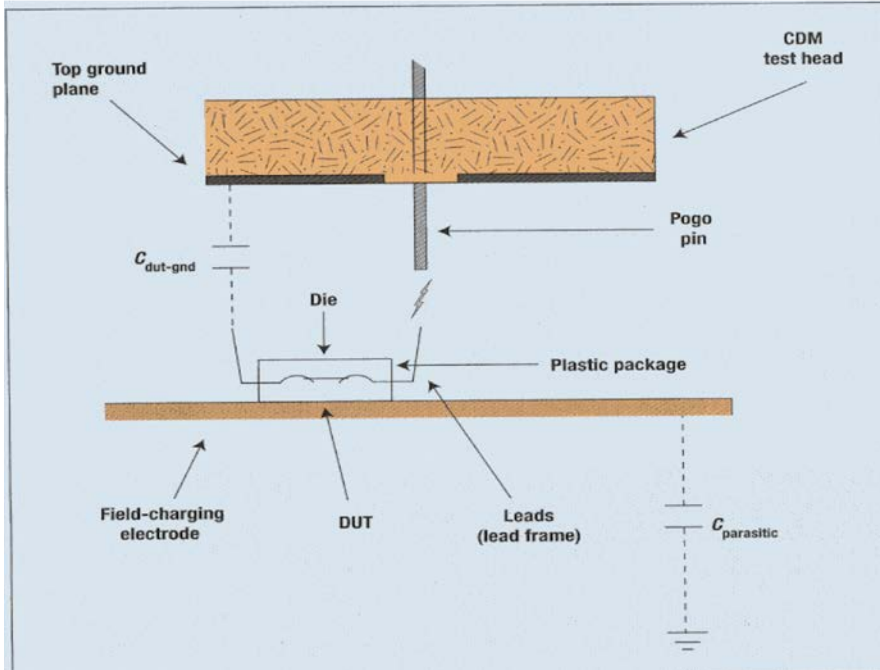


Figure 7. Device capitance for R-CDM test simulators.

This small difference in SDM test-system capacitance can easily explain why the SDM tester is unable to detect any difference in failure voltages due to large changes in package capacitance.

Second-Generation SDM Test System

Can the commercially available SDM test systems continue to be used today? The answer is yes, if overstressing an IC is acceptable. In fact, for many users, the SDM test system has become a valuable tool in isolating CDM-sensitive pins and then in verifying the success of redesigns. The simulator successfully identifies sensitive device pins in some, but not all, CMOS technologies. The IC failure signatures frequently do agree with R-CDM failures, but again, not for all CMOS technologies.

Can the existing SDM simulator be expanded to meet the demand for testing high-pin-count devices? The answer is both yes and no. Attempts to increase the physical size of the test system to increase the pin count have resulted in even larger background capacitive and inductive elements. Other efforts, including customized test-socket boards that divide the high pin count into smaller pin subgroups, have been more successful since they do not add more background tester parasitics.

The design of the existing SDM simulator is unique. The amount of charge stored in the test system is distributed through a complex network of test-fixture boards, sockets, relays, and other unique RLC elements.[15] Changing any of these elements, like replacing a test fixture and socket board, will modify the amount of charge stored in the system. Any discharge currents measured from an IC will be a distinct product of this distributive-charge network. Consequently, writing a standard test method for this type of ESD test equipment is impossible.

A standard test method must be written in general terms, so that any test equipment manufacturer can build a similar system. The existing SDM design introduces parasitic capacitive and inductive elements that must be duplicated in order to generate discharge current waveforms with similar time-amplitude characteristics. If these waveforms cannot be duplicated by other SDM test equipment, then the SDM failure voltage will not correlate. Consequently, the unique properties of the SDM test system prohibit the development of another system.

Conclusion

In summary, this type of SDM test system cannot be fundamentally improved. Consequently, a new design for S-CDM test systems must be developed. In fact, the need increases as the number of IC pins continues to increase and the pin pitch continues to decrease. If a second-generation S-CDM test system were to be built today for the purpose of correlating with R-CDM, the new system would need to include and achieve the following:

- Eliminate or significantly reduce the discharging of tester parasitic capacitive elements while the DUT is discharged.
- Give the DUT a known ground-capacitance value by replicating the R-CDM ground-plane capacitance effects.
- Generate discharge-current waveforms with similar time-amplitude characteristics observed in the R-CDM test systems.
- Measure the discharge current through a low-inductance resistor (identical to the method used in the ns-CDM test method).[6]
- Establish correlation between S-CDM and R-CDM testers, to accelerate industry acceptance.

Can a second-generation S-CDM system that can meet these requirements be built? This is the current challenge for ESD test-equipment manufacturers. To date, the IC manufacturing community is waiting for someone to design and build a better S-CDM test system. Meanwhile, the ESDA Working Group 5.3.2 is developing a standard-practice document scheduled for release in early 2002. This document will recommend general test procedures to use with current SDM test systems to obtain meaningful information.

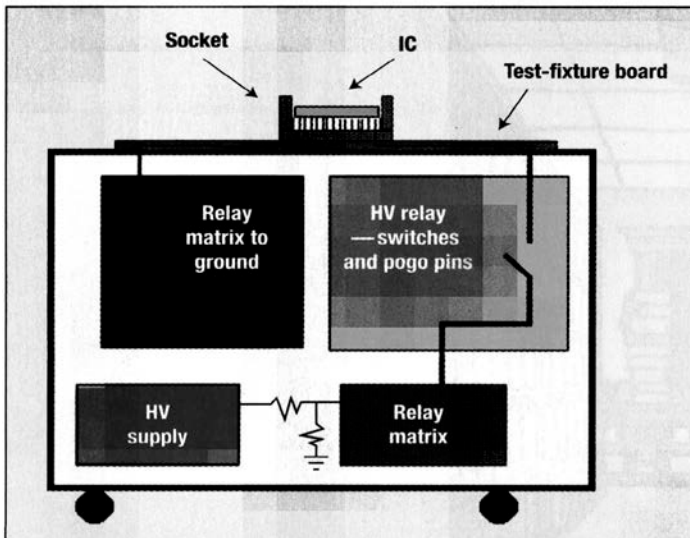


Figure 8. SDM tester parasitics can be defined as variable and fixed RLC parasitic elements.

Acknowledgments

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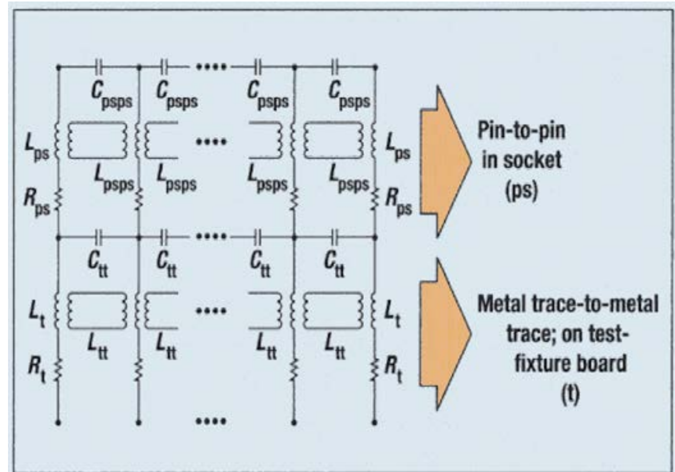

Figure 9. Variable external RLC parasitics.

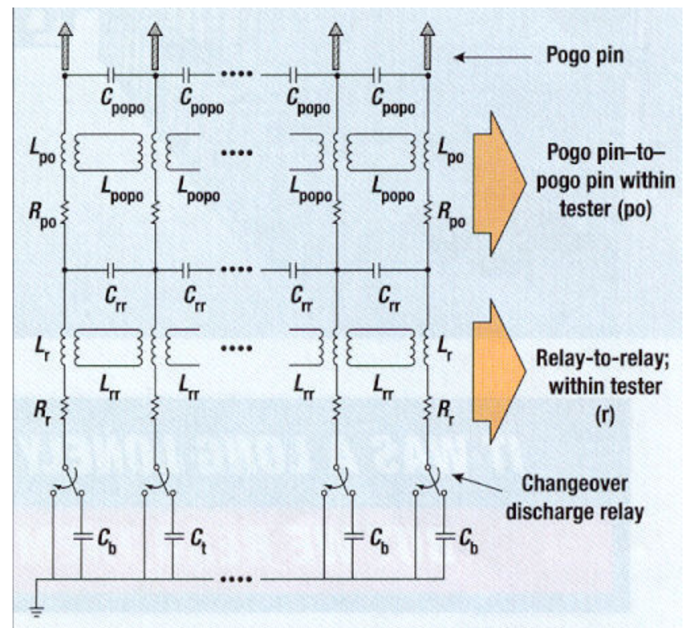

Figure 10. Fixed internal RLC parasitics to SDM tester.

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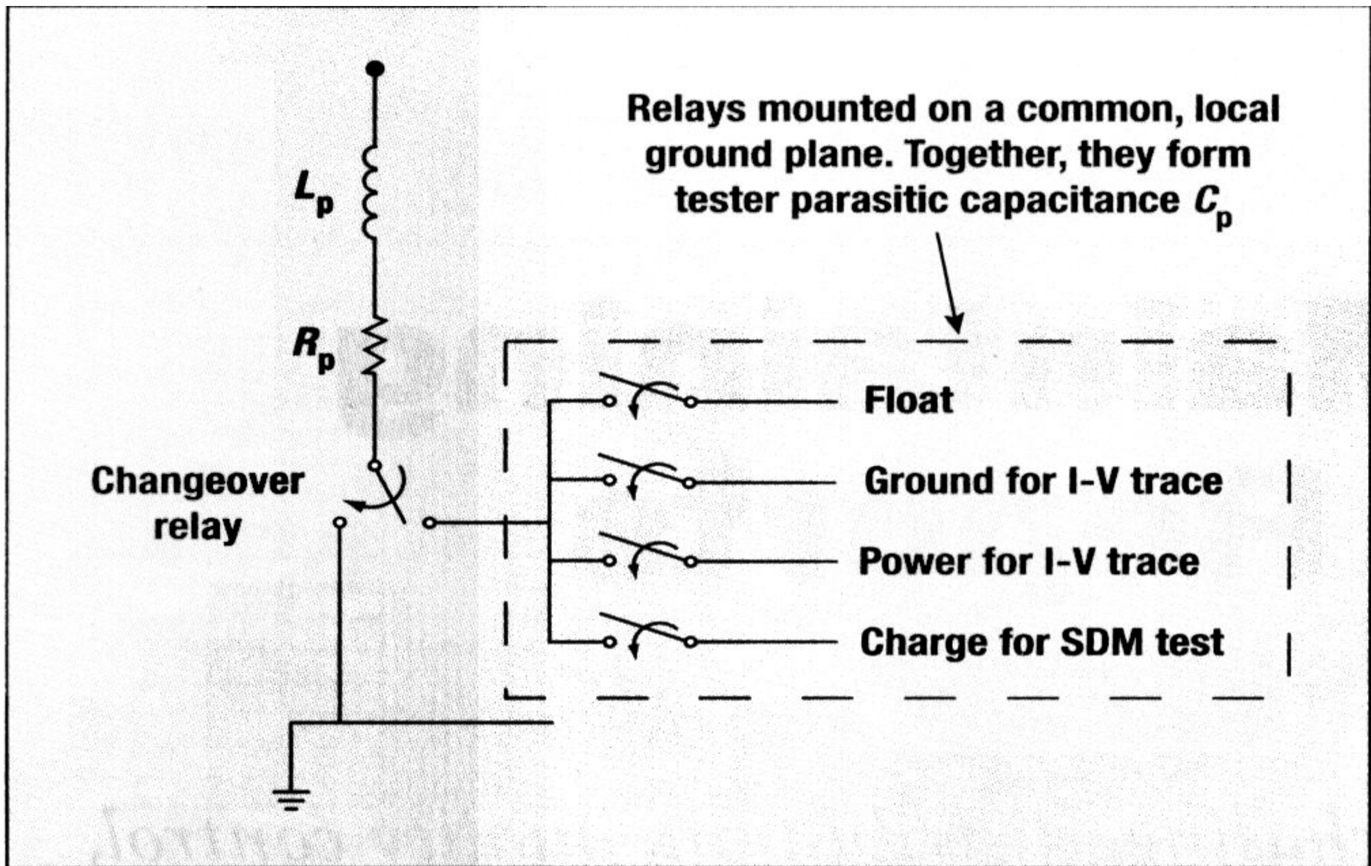

Figure 11. Simple model for the SDM tester parasitic elements for each test socket pi n. Each pin has parasitic inductance (Lρ), resistance (Rρ), and capacitance (Cρ).

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