Modeling CDM Failures in High-Voltage Drain-Extended ESD Cells

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Abstract – Device simulation and physical modeling are used to explain the location and feature size of gate oxide defects seen post CDM testing. By comparing the model with defect measurements, a value for oxide breakdown voltage is obtained that is 1.6 times the DC value, a result that is also in agreement with device simulation. Finally, the model is used to suggest methods for improving CDM performance.

I. Introduction

Lateral drain-extended NMOS devices are frequently used for electrostatic discharge (ESD) protection in analog and mixed-signal applications where rated voltages are 80V or larger. Although the human body model (HBM) performance of these devices has been discussed in the literature, their charged device model (CDM) behavior has received little attention.

This paper has two themes, one dealing with I-V behavior and device simulation, and a second, describing a physical model that accounts for observed features of fail sites revealed by physical analysis of packaged units that were CDM tested.

The main intent of the paper is to enhance the understanding of CDM behavior in high-voltage ESD cells and to suggest methods of improving performance.

A. Overview of Test Results

The cell discussed in this paper is a grounded-gate lateral DENMOS designed to provide protection for 80V pin applications. Although this cell provides more than adequate HBM protection, field-induced CDM testing above 300V results in damage that appears electrically as excess gate-drain leakage current in the range of 30 to 80 μA at rated voltage.

Another departure from HBM behavior is that the voltage threshold for the onset of CDM failure shows no clear dependence on the polarity of the CDM charging voltage.

II. TLP Measurements

Fig. 1 shows a measured *I-V* characteristic for the 80V gg-denmos cell. Wafer-level measurements are made using a transmission line pulse (TLP) system with 100ns pulses and 10ns rise time.

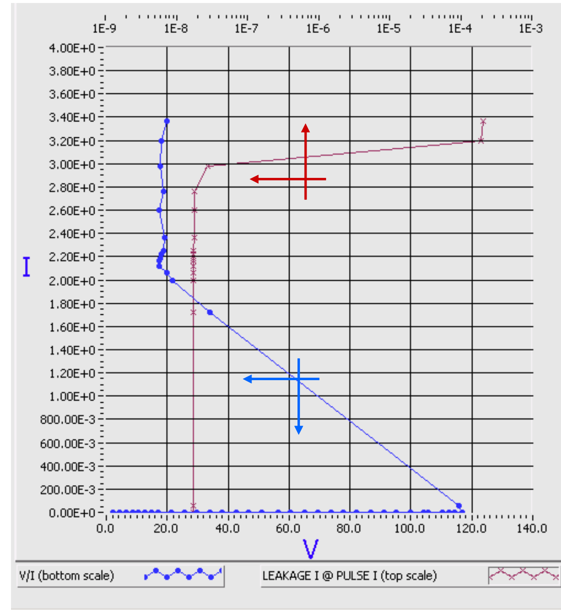

Fig. 1. Measured TLP *I-V* charactersitics of the 80V gg-denmos cell. Pulse width is 100ns (Measured using a Barth TLP system).

Drain current is plotted vs. drain-source voltage and also vs. DC leakage current that is measured after each pulse. Leakage current is plotted on the horizontal scale at the top of the plot in the usual

TLP format. The plot shows a trigger voltage *Vt1* of 116V, a holding voltage *Vh* of 18V, and a failure current *It2* of 3A. Using a 2kV/1A conversion factor, this corresponds to a 6 kV HBM failure level, which is more than adequate for the application.

A. VFTLP Measurements

Because the CDM discharge occurs over a much reduced time scale compared to 100ns (*e.g.* 1ns or less), it makes sense to look at TLP *I-V* data for shorter pulse times. Fig. 2 is a VFTLP *I-V* plot for 3ns pulses. It can be seen the trigger voltage is increased to about 135V and the holding voltage is increased by more than three times. We can ascribe both increases to the relatively long base transit time of the parasitic npn. That is, it takes some time for excess base charge to build up in the npn due to its relatively wide base.

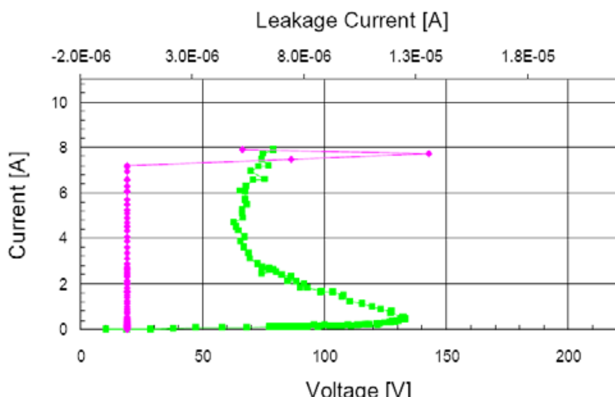

Fig. 2. VFTLP measurments for a pulse time of 3ns. Measurements are on a packaged part with discharge at the protected pin.

Fig. 3 is similar Fig. 2 but the pulse time is reduced to 1ns. Although the I-V plot is noisy, it appears that the average current increases with applied voltage. The current increase can be ascribed to impact ionization, but it should be noted that there is no snapback, that is, turn-on of the npn. The lack of snapback is due to the time required (several ns) to inject charge into the npn base region. This behavior is approximately what we can expect during a CDM discharge and it provides a basis for the device simulation described in the next section.

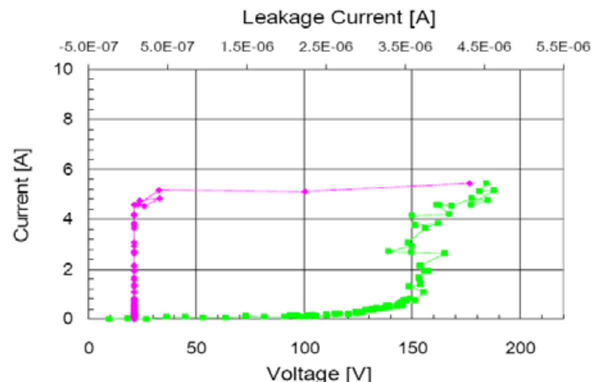

Fig. 3. VFTLP measurements for a pulse time of 1 ns. This data and the data Fig. 2 was obtained using a Hanwa VFTLP system.

III. Device Simulation

Fig. 4 shows a schematic cross-section of the grounded-gate DENMOS. For the cell design considered in this paper, FCDM testing in excess of 300V produces oxide failure sites at the bird's beak as indicated in the figure. The DENMOS under study is processed using bonded SOI wafers, having a buried oxide of 1 µm and silicon thickness of 7 µm.

A. Voltage ramp

Although an actual CDM discharge gives oscillatory current and voltage waveforms, we can approximate the initial stages of this event by using a rapidly rising voltage ramp applied drain to source. The exploration of device behavior is limited to times in the vicinity of this ramp.

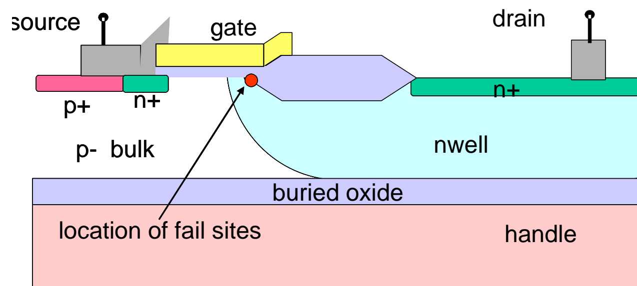

Fig. 4. Cross-section of the SOI grounded-gate DENMOS.

Fig. 5 shows the applied voltage ramp of 500V with 100 ps ramp time. The ramp time is not critical as long as it is short enough. A resistance is added in series with the drain to approximate the packaged die and its discharge path. The device

width is 200 µm, giving an equivalent resistance of 50 ohm and a short circuit current of 10 A.

The point in Fig. 5 at 80 ps corresponds to the equipotential cross-section plot of Fig. 6. The depletion layer has partially spread into the channel region under the gate oxide and some impact ionization current is flowing. Bipolar action is not yet sufficient to reduce *Vds* significantly.

The cutline in Fig. 6 is just under the gate oxide and crosses into field oxide at the bird's beak. By looking at voltage profiles along this line, we can get an idea how voltage builds up across the gate oxide.

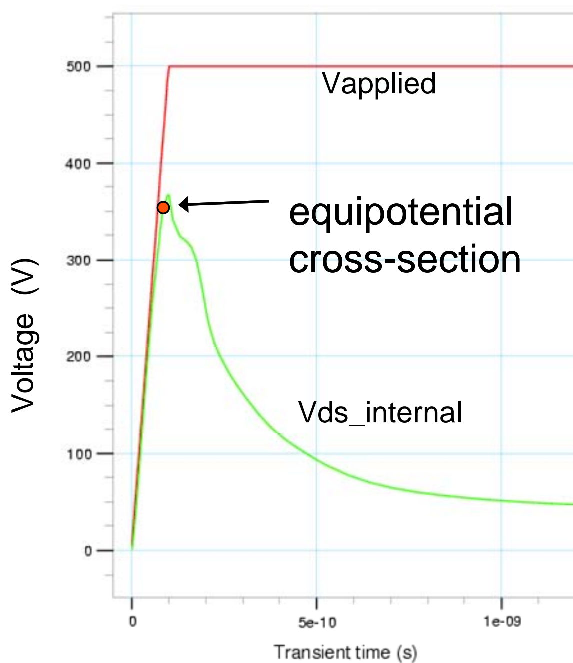

Fig. 5. Voltage waveforms used for device simulation. The initial part of the waveform applies to a CDM discharge.

A plot of the voltage profiles for several time points is shown in Fig. 7. It can be seen that the voltage at the bird's beak is initially near zero (35 ps), increases to a peak of 115 V at 144 ps, and then decreases, reaching near zero at 300 ps. Since the gate is at zero volts, we can see that the maximum voltage across the gate oxide is always occurring at the bird's beak, agreeing with the location shown in Fig. 4.

The voltage profiles of Fig. 7 show a "dip" upon exiting the silicon just beneath the gate and entering the thick oxide region. The dip in the voltage profile is mainly due to influence of the polysilicon gate, which acts as a field plate and tends to bend the equipotential lines downward. This behavior can be demonstrated by following the equipotential lines in Fig. 8. This figure also shows that the electric field in the oxide near the bird's beak is exceeding 3e7 V/cm.

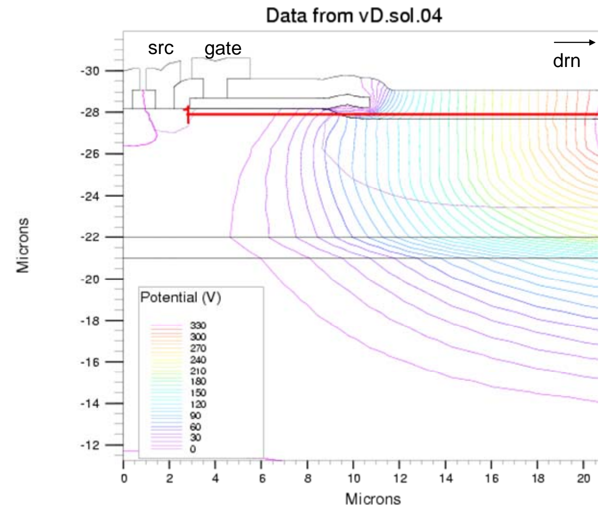

Fig. 6. Cross-section showing equipotentials for the point indicated in Fig. 5 (t=80 ps). Contours are spaced by 10V. The drawn cutline extends through the channel region and into field oxide.

B. Voltage profiles for different times

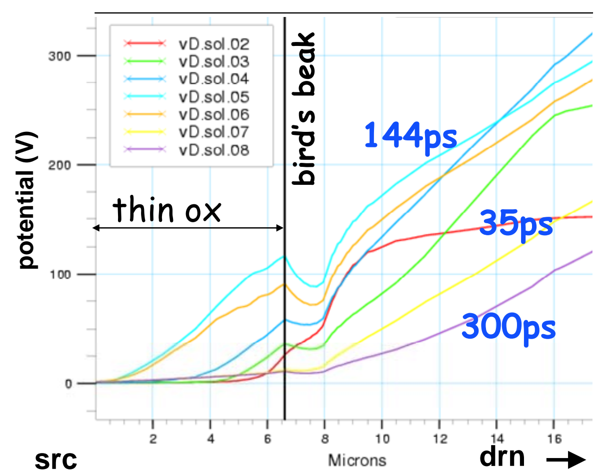

Fig. 7. Voltage profiles along the cutline of Fig. 6, for different time points.

Fig. 9 shows the time-dependent behavior of the bird's beak voltage corresponding to the plots of Fig. 7. As indicated, the DC breakdown voltage of the gate oxide is 45V. The peak voltage is about three times this value and is likely to lead to breakdown.

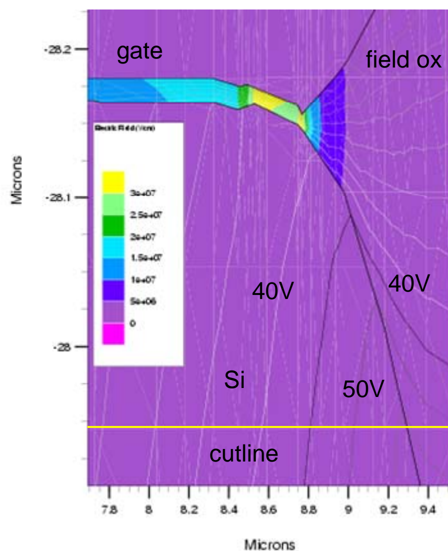

Fig. 8. Close-up of bird's beak region showing equipotential and electric field contours (t=80 ps). Note the high field region in the gate oxide.

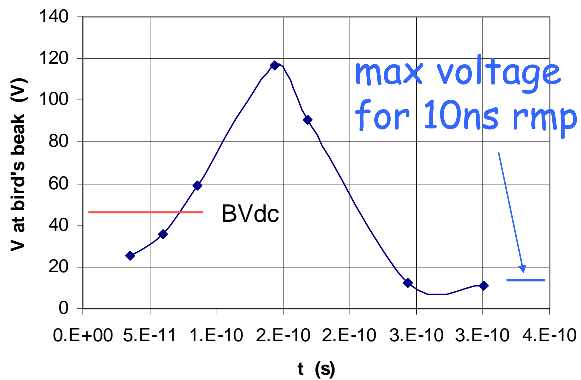

Fig. 9. Voltage at the bird's beak vs. time for the profiles of Fig. 7. DC breakdown voltage is indicated.

With longer ramps, the peak voltage will decrease. For example, for a 500V, 10ns ramp the maximum voltage decreases to 15 V. This explains why CDM testing can degrade the gate oxide and HBM does not.

The same type of analysis has been carried out but with a negative 500V ramp. Again, the bird's beak sees the greatest oxide stress with profiles similar to those of Fig. 7 but with the opposite slope. Fig. 10 shows a plot of the bird's beak voltage for the negative ramp case. The peak voltage is about 20 percent less than obtained with the positive ramp. In this case, the waveform is analogous to that in the "forward recovery" process of a diode.

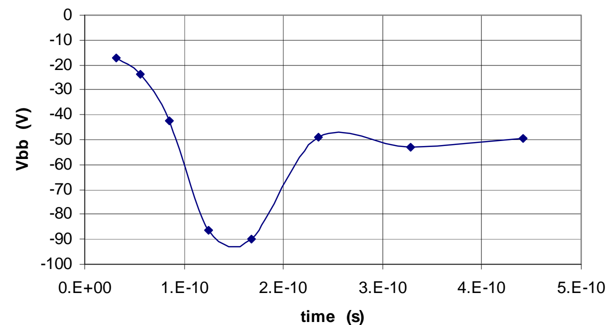

Fig. 10. Voltage at the bird's beak for a negative 500V, 100ps ramp applied drain to source.

In summary, device simulations show that gate oxide breakdown is likely to occur at the bird's beak. The peak voltage across the oxide is approximately 115V for a 500V ramp. The FCDM threshold for failure generation is approximately 300V. If we scale the peak voltage of 115V by the ratio 300/500, the peak voltage across the oxide corresponding to the CDM failure threshold is 69 V. In the next section, we show that this value agrees well with the breakdown voltage obtained by physically modeling the formation of oxide defects, a totally different method.

IV. A Physical Model of Defect Formation

Failure analysis can provide very useful information about oxide defect formation. Fig. 11 shows a top view after 500V FCDM testing. The top layers; oxide and metal plus polysilicon gate have been removed. Oxide defects are revealed by etching. The damaged regions are nearly semi-circular in shape. These defects are all located at the bird's beak and are spaced fairly uniformly along this line on both sides of the source window.

A. Constructing the Model

Fig. 12 shows a close-up from Fig. 11 where a number of semi-circular melt sites are visible along the bird's beak edge. Fig. 13 gives a schematic view of the polysilicon gate, showing uniformly spaced melt sites. The spacing between sites is s and the melt radius is r_m. The gate forms

a top electrode of a capacitor and is at ground potential. The other plate is the silicon under the gate oxide. This plate is assumed to be at uniform potential. During the oxide breakdown event, current flows from the silicon up through the melt sites and then out through the top polysilicon to the grounded source.

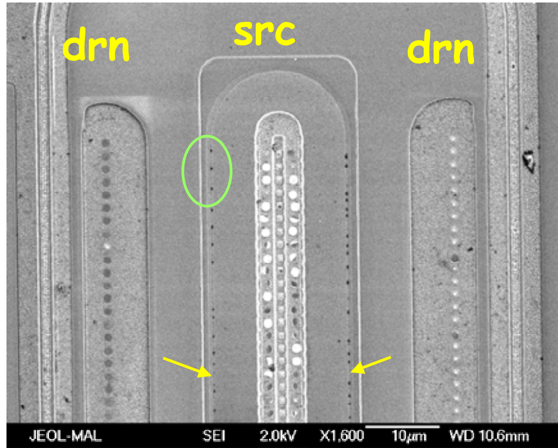

Fig. 11. Post failure analysis from 500V FCDM test. Top view showing center source and outside drain regions. The bird's beak is indicated by the arrows. Fig. 12 shows a close-up of the area indicated by the oval.

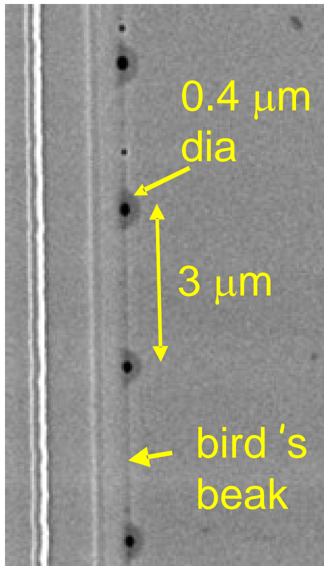

Fig. 12. Close-up of gate oxide defects from Fig. 11.

B. Modeling Current Flow

Fig. 14 indicates the current flow behavior for a single melt site. We can approximate current flow within the polysilicon sheet as being equivalent to the electrostatic potential for an infinite array of line charges [1], [2]. In this case, the melt radius *rm* acts as an equipotential. At the same time, we approximate the melt region as a lumped resistor *Rm* as indicated in Fig. 14. This figure diagrams current flow in the vicinity of the melt site. *Rsp* is the effective spreading resistance between melt site and the source contact.

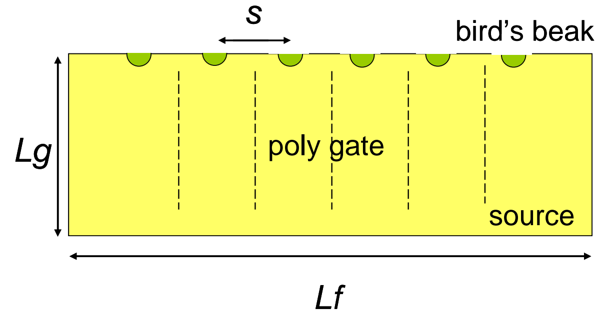

Fig. 13. Top view of gate showing melt sites and gate dimensions. The dashed lines indicate individual cells used to model melt site formation.

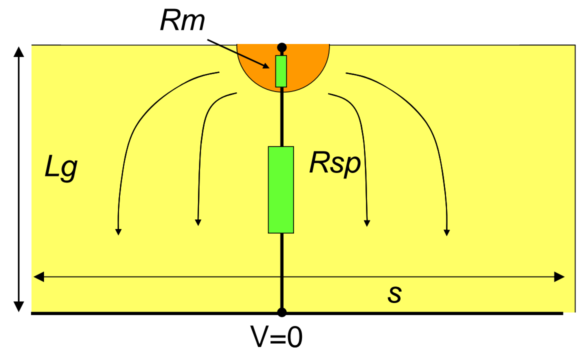

Fig. 14. Single melt site cell showing lumped spreading resistance and melt resistance.

From the potential solution, we find

$$Rsp = \frac{Rs}{\pi} \cdot ln(\frac{\pi \cdot s}{rm}) \qquad (1)$$

where *Rs* is the polysilicon sheet resistance. The resistance given by (1) is for the semi-infinite case and is twice the value that would apply for current flow in an infinite sheet.

Fig. 15 shows a circuit model used to represent electrical behavior at the melt site. Although oxide degradation and oxide breakdown are actually a series of complex events, we approximate oxide breakdown *I-V* behavior by a switch in series with a fixed resistor *Rm.* This simplification is made because we are interested in failure analysis aspects rather than details of gate oxide degradation.

The capacitor in Fig. 15 is equal to the gate-channel capacitance of one finger *Cg*, divided by the number of melt sites *Nm*. The spacing *s* is equal to the finger length *Lf* divided by *Nm*.

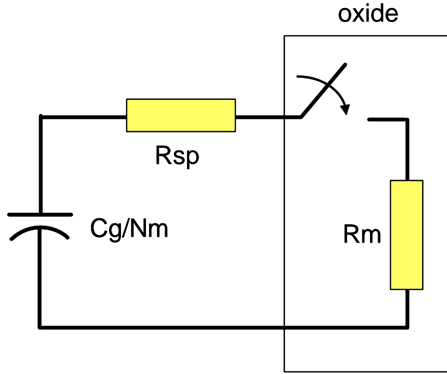

Fig. 15. Circuit model for a single melt site.

C. Energy Balance

The energy available to raise the melt site temperature is

$$Eam = Vox^2 \frac{Rm}{Rm + Rsp} \cdot \frac{Cg}{2 \cdot Nm} \qquad (2)$$

where *Vox* is the voltage on the capacitor at breakdown.

Because of the short times involved, we can assume adiabatic heat flow at the melt site. Using the volume defined by the semi-circular area of radius *rm* shown in Fig. 14, and the gate oxide thickness *xo*, gives the melt energy of

$$Em(rm) = (Tm - Ta) \cdot cp \cdot den \cdot \frac{\pi}{2} \cdot rm^2 \cdot xo \qquad (3)$$

where *Tm* is the oxide melting temperature (1735 C), *Ta* is the initial ambient temperature, and *cp* and *den* are the oxide specific heat and density respectively. The gate oxide thickness is 45 nm.

In this work we view oxide breakdown as a negative resistance phenomenon. That is, current tends to localize and expand the melt radius *rm*. Melt growth is limited by power lost in the spreading resistance *Rsp*. Maximum growth will occur at maximum power transfer, when *Rsp* matches *Rm*, which is the assumption made here.

Using (2) and (3) we obtain an equation for the number of melt sites *Nm.*

$$Nm(rm) = \frac{Vox^2 \cdot Cg}{4 \cdot Em(rm)} \qquad (4)$$

Measured and calculated *Nm* are compared in the next section.

V. Results

A. Oxide Breakdown Voltage

Fig. 16 shows plots of (4) using different oxide breakdown voltages. The best fit to measured data of *Nm*=44 and *rm*=0.2 μm is for *Vox* = 70V. It is interesting that this voltage is very close to the value obtained from the device simulation of Section III. Considering the approximations made in the physical model, this good agreement seems fortuitous, but it is the result obtained.

The increase in oxide breakdown voltage over DC values is also consistent with measured data reported by a number of authors [3]. [4], [5], [6]. Comparing the breakdown voltage of 70V to the measured DC breakdown of 45V gives a ratio, equal to 1.6, the same value reported in [6] for 1 ns pulses and 20 nm oxide thickness.

Please note that the plots of Fig. 16 are independent of any particular values of *Rsp* or *Rm.* The only condition is that these resistors be equal.

B. Melt Resistivity

The melt resistor *Rm* can be approximated by a simple one-dimensional model, which assumes a uniform melt resistivity ρm and semi-circular contact areas, as indicated in Fig. 14.

$$Rm(\rho m, rm) = \rho m \cdot \frac{xo \cdot 2}{\pi \cdot rm^2} \qquad (5)$$

Equating *Rm* to *Rsp* and using (1), we can solve for the melt resistivity

$$\rho m(s, rm) = \frac{\pi \cdot rm^2}{xo \cdot 2} \cdot \frac{Rs}{\pi} \cdot ln(\frac{\pi \cdot s}{rm}) \qquad (6)$$

Fig. 17 shows a plot of calculated melt resistivity for two different values of spacing. Using the measured *rm* value of 0.2 μm suggests that melt resistivity is about 4 mohm-cm. This is a very small value, for example, in comparison to the room temperature resistivity of quartz (e.g. 10^{20} ohm-cm).

AC measurements of molten glass [7] report a resistivity 5 ohm-cm which is still much larger than the 4 mohm-cm obtained in Fig. 17. Further work is needed to understand what this low value of resistivity means from the perspective of the oxide breakdown process.

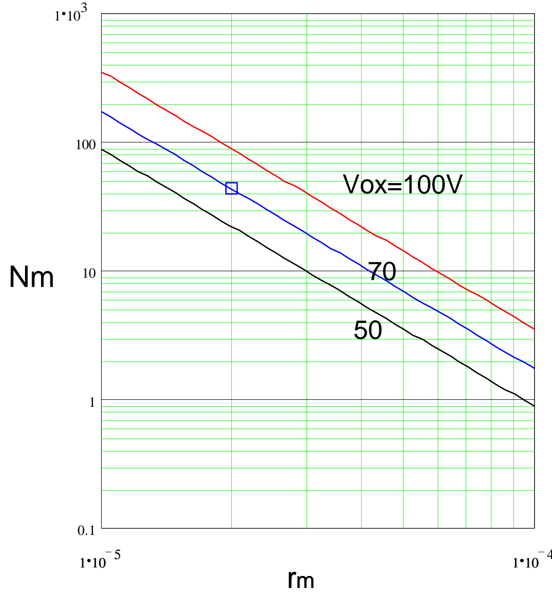

Fig. 16. Predicted number of melt sites vs. melt radius using (4) with different oxide breakdown voltages. The data point indicates the measured number of melt sites (44) and melt radius (0.2 μm).

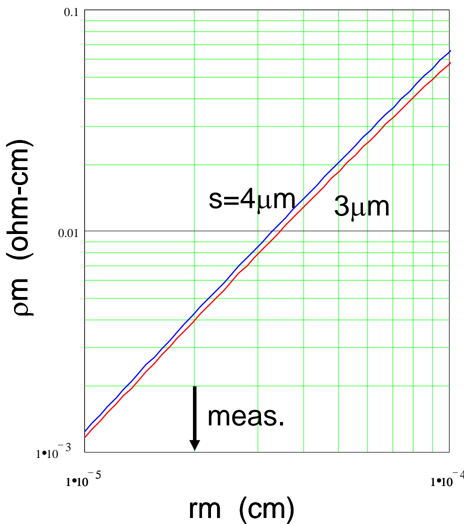

Fig. 17. Calculated melt resistivity vs. melt radius for a spacing of 4μm and 3μm. Measured radius is indicated.

VI. Discussion

How can we use these results to improve CDM performance? Two possibilities can be suggested:

1. Reduce the channel length in comparison to the total drain-source spacing. This will reduce the fraction of total voltage appearing at the bird's beak and reduce the likelihood of oxide breakdown.
2. Add a resistance *Rex* in series with the gate. This means adding an *Rex* term in the denominator of (2). This will reduce the energy available to form the melt site and as a result, *rm* will be reduced, according to (3). The added resistance needs to be large enough to ensure that *rm* is significantly less than the gate oxide thickness *xo*.

VII. Conclusion

Device simulation and physical modeling have been used to develop a relatively simple thermo-electric model that explains the physical features exhibited by CDM failure sites in high-voltage DENMOS ESD cells.

Improved CDM performance can be achieved by reducing the peak voltage seen at the bird's beak during the ESD event or by reducing the current available to form melt sites. Two methods have been suggested for achieving this enhanced performance.

VII. References

[1] E. Weber, *Electromagnetic Fields,* John Wiley, 1950, p. 294.

[2] L. V. Bewley, *Two-Dimensional Fields in Electrical Engineering,* Macmillan, 1948, p. 52.

[3] M. Bridgwood, "Breakdown mechanisms in MOS capacitors following electrical overstress," Proc. EOS/ESD Symposium, 1986, pp. 200-207.

[4] Y. Fong, C. Hu, "The effects of high electric field transients on thin gate oxide MOSFETS," Proc. EOS/ESD Symposium, 1987, pp. 252-257.

[5] J. Wu, P. Juliano, E. Rosenbaum, "Breakdown and latent damage of ultra-thin gate oxides under ESD stress conditions," Proc. EOS/ESD Symposium, 2000, pp. 287-295.

[6] H. Gieser, M. Haunschild, "Very-fast transmission line pulsing of integrated structures and the charged device model," IEEE Trans. on Components, Packaging, and Manufacturing Technology, Part C, v. 21, Oct. 1998, pp. 278-285.

[7] C. Simonnet, J. Phalippou, M. Malki, A. Grandjean, "Electrical conductivity measurements of oxides from molten state to glassy state," Rev. Sci. Instrum., v. 74, May 2003, pp. 2805-2810.