

TLP and VFTLP Testing of Integrated Circuit ESD Protection

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This paper presents electrical methods used to measure and analyze the operation of ESD protection circuits built into every lead of an Integrated Circuit (IC). These circuits clamp voltage threats to sensitive core circuits which enter through each connections to the outside world. Representative samples of each IC are tested for their ESD immunity level to insure a minimum level of protection. Different standards specify electrical waveform parameters which simulate voltage levels, source impedances, and waveforms from different ESD source threats. ESD testing identifies immunity levels on IC's by a simple pass or fail result; but provides no additional data on the failure cause.

ESD occurs when a charge that is stored in a capacitive element, discharges into a pin (or lead/ball) of an integrated circuit. There are a number of fundamentally different ESD threats to core circuits. The two basic threats are Human Body Model (HBM) which lasts 150 nanoseconds and the Charged Device Model (CDM) which lasts only a nanosecond or two.

ESD protection circuits clamp ESD voltages to an acceptable level and shunt their current to ground. To protect core IC operating circuits, the voltage clamping circuit must turn on at a voltage slightly above that of the signal/data level. ESD protection circuits are located at the outer edges of an IC chip where its leads connect to the outside world. They are placed at the bond pad or directly under it to save expensive silicon surface space. Their only purpose is to protect the operating core circuits by clamping the ESD voltage to harmless levels, and shunting the ESD current harmlessly to ground.

HBM/TLP Testing

The HBM discharge is a simple RC exponentially decaying waveform which is 150 ns long at its 1/e amplitude as shown in figure 1.

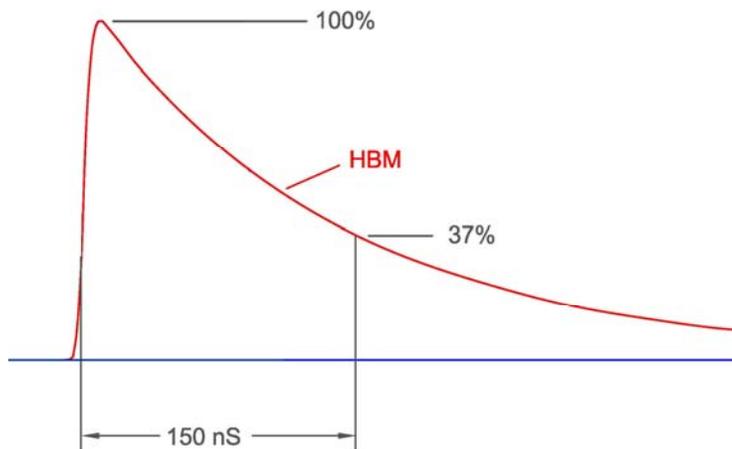


Figure 1. HBM/TLP Test Pulses

It is produced by a capacitor of 100 pF charged to the desired test voltage. It was the original ESD test and simulates that of a human standing above a conductive ground. The discharge resistance is 1500 ohms which simulates that of the finger and skin. Although

human hands seldom assemble integrated circuits today, this test remains the fundamental ESD energy dissipation test required for general ESD immunity. Each pin is tested to every other pin on the IC as a pair; although some exceptions are made for power pins connected together with minimum resistance. Optimum HBM protection circuits provide the required immunity level and pass the threat current while dissipating its energy in the minimum area dedicated to ESD on the chip. Standards identify how the ESD test is to be made, while test levels determine the device's ESD immunity level. It is a pass or fail test that the pins of an IC must withstand to meet immunity specifications

While real world ESD can have sub-nanosecond risetimes, the risetime of HBM test pulses is specified to be between 2 ns and 10 ns. HBM tester requirements for rapid switching the test pulse between any two pins in a 1000 pin matrix can cause waveform distortion at the 2 ns risetime. Therefore most HBM test waveforms typically operate near 10 ns rate of rise.

TLP testing was invented in 1984 at INTEL [1] as an analysis method to measure the electrical characteristics of ESD protection circuits. TLP is an abbreviation of Transmission Line Pulse method of generating a test pulse. It is produced by discharging a charged transmission line to produce a flat top pulse. The Transmission Line Pulse test waveform is compared with the HBM test pulse as shown in figure 2.

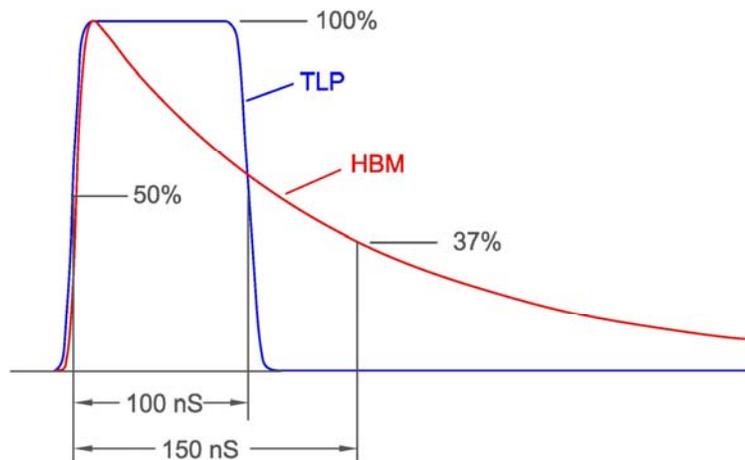


Figure 2, HBM and TLP test pulse waveform comparison

TLP testing began with 100 ns long rectangular test pulses and has become the standard pulse length. At the same 100% peak current amplitude, the TLP test pulse should theoretically be 75 ns long. However measurements on diodes have shown that 80 ns long TLP test pulse causes the same peak current failure levels as the HBM test pulse. TLP has about 25% more energy than an equal peak current HBM test pulse.

The TLP test pulse can be produced with minimal parasitic distortions to the test pulse waveform. It is relied on for accurate failure energy level measurements when questions arise about HBM test level failures.

The TLP test takes a few seconds for the digitizer/computer to average many data voltage, current, and leakage current points for high accuracy. Averaging reduces the digitizer noise and provides an improved signal to noise ratio. New ESD Test Structures

can be put on scribe lines or test wafers to evaluate the effectiveness of new designs or next generation geometries.

The same test pulse risetimes are used in TLP and HBM to exercise the turn-on properties of the Device Under Test (DUT) in the similar manner.

Waveform errors inherent in the HBM tester construction occasionally produce different failure levels when the same device is tested on different HBM systems. The cleaner TLP delivery system produces minimal waveform parasitics that do not affect DUT turn-on characteristics. This test pulse is delivered to by two needles which connect directly to ESD circuits on wafer or to packaged parts. The test pulse is connected directly to the DUT on bare silicon through high speed two needle connections as fast as 0.2 ns risetime with minimal distortion. It is applied to the silicon clamping circuit to measure the voltage (V) across it and the current (I) through it. By continuously increasing the amplitude of the pulse voltage applied to the silicon, the device's complete I/V characteristics are identified and can be plotted. We sometimes identify TLP as a "pulsed" curve tracer.

The I-V data point for each of multiple test amplitudes are displayed on a plot as shown below in figure 3.

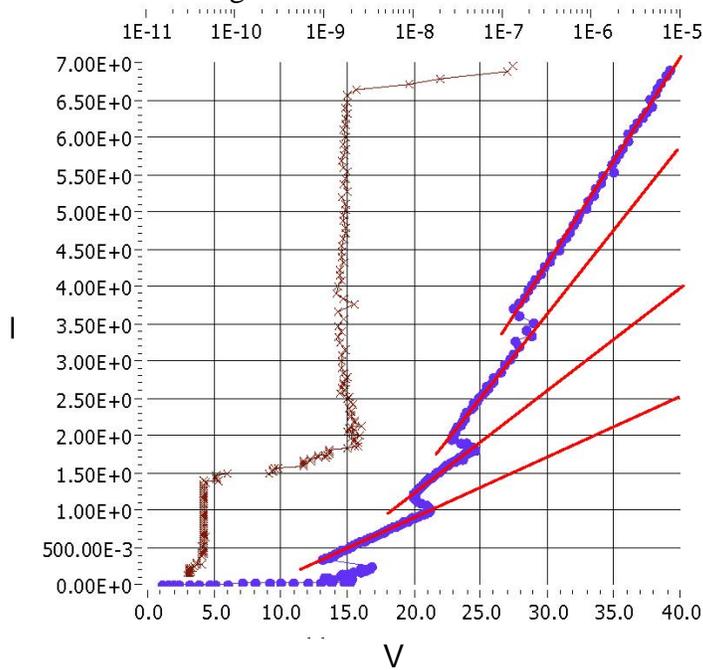


Figure 3. TLP data displays dynamic resistance characteristics

The device voltage and current from each TLP pulse are shown as a blue data points on the I-V plot. The leakage current, typically measured at its operating voltage after every test pulse, is shown as brown X points on the curve. Its values are identified on the multiple log scale at the top of the plot and each is aligned with the preceding pulse current value on the left. Each data point takes a few seconds, so a complete I-V plot like this can take 2 to 6 minutes. This ESD protection element was a device that turns on and begins to clamp the external ESD voltage to protect the core circuit at about 15 volts.

When the current indicated by blue dots circuit reached about 250 mA at 17 volts, one of the multiple conductive circuit fingers turned on with a snap-back action. That dropped the circuit's voltage to 13. The current increased smoothly until it reached 1 amp and 21 volts when another of the either 4 or 8 conduction circuit fingers on the silicon snapped back to 20 volts. ESD voltage clamps are typically made with 2ⁿ silicon fingers in parallel to spread the current to many different paths. As each of these fingers began conduction they share the current and their combined dynamic shunt resistance is reduced. This continued until at 6.5 amps where failure, as indicated by the leakage current increase occurred somewhere on the silicon circuit. At that peak current the circuit's leakage current increased from 2e-9 to about 1e-7, indicating a major failure. While there was an almost 2 order magnitude of current increase in leakage current between 1.5 and 2 amps of test pulse current, it did not seem to affect the turn on of the multiple fingers. This data allows the ESD designer to know where the leakage increased so he can determine its cause. The increase from 3e-11 to almost 2e-9 could shorten battery life in a hand held unit or increase the thermal load on a table top unit.

Minor increases in leakage current measured after small test pulse amplitude increases, can provide detailed information on impending failure or inception of damage. Latch up can also be identified when the holding voltage of the circuit is below the operating voltage or when it drops below operating voltage at temperature. The TLP data also measures the maximum voltage that must not exceed the gate oxide voltage limit. Special osmium alloy tip needles are used which do not form an insulating/resistive oxide as tungsten does. Maintaining very low contact resistance to aluminum pads is necessary when the ESD circuit itself has one or two ohm dynamic resistance. TLP testing of packaged parts is used when problems arise or the customer has ESD failure issues. It is also used to determine which HBM test result is correct when different HBM testers indicate different failure levels. Test systems allow TLP testing to be terminated before significant damage occurs which can obscure the exact silicon failure location. TLP provides significant detail on silicon circuit operation which is far more sensitive than the Go, No-Go failure information in HBM testing. I tell potential customers that if they are in the ESD design business they have to buy, build, borrow or steal a TLP system to be cost and time effective in their ESD design.

TLP testing can also provide Safe Operating Area (SOA) information on DMOS transistors. The TLP pulse length can be increased to microseconds to measure electrical characteristics at different gate bias levels to provide a family of curves for a specific pulse length. By adjusting the gate bias to certain values Safe Operating Area (SOA) measurements can be made for special power level transistors that operate in pulsed modes. The electrical engineering methods used to produce TLP test pulses are covered in many papers published on the Barth Electronics website [2] and by the Electro Static Discharge Association [3]

CDM/VFTLP Testing

The other ESD sensitive elements in MOS integrated circuit design are gate oxides which fail from excess voltage during a very short pulse or period of time. It is identified as the CDM test method which produces extremely fast rising discharges. This event discharges the capacitive charge on an integrated circuit through one pin or ball. The failure level of each type of gate insulator and its thickness depends on its Time

Dependent Dielectric Breakdown (TDDB) limitations. The time to failure can be years at operating voltages to picoseconds for extremely short pulse lengths. The high speed CDM discharge occurs when a metal pin or lead on an electro-statically charged IC package discharges to a metal ground plane.

Higher pulse speeds possible with TLP coaxial cable delivery system have evolved into Very Fast TLP (VFTLP). It uses shorter pulses with faster rates of rise which simulate the much faster Charged Device Model (CDM) threat and test. Much faster current and voltage probes are used to monitor DUT current and voltage ESD protection circuits found in this technology. Analyzing the sub-nanosecond circuit operation on bare silicon is a unique measurement process. Specially designed low inductance switches placed in a constant impedance coaxial housing preserve the fastest possible risetime. When used with short transmission lines they produce the short VFTLP pulses. We produce pulses of 1, 2, 5, 10 nanoseconds in length. The test pulse risetimes are selectively slowed to produce 100, 200, 400, 600, and 1000 ps risetimes which simulate the high and medium speed ESD threats and test methods.

Accurate measurements of time vs. conductance effects provide very useful information on high speed ESD threat effects for different ESD specifications of system interface connection methods and their protection.

The CDM discharge current waveform and the VFTLP Test waveforms are shown in figure 4.

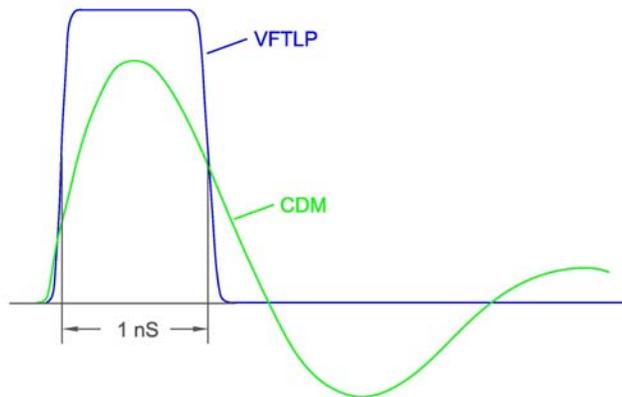


Figure 4. The typical CDM discharge current waveform and the VFTLP test waveform.

The very low resistance of metal discharge electrodes produces a very fast ESD voltage threat at higher currents than HBM. Discharges between metal electrodes have been measured to be faster than 0.1 nanosecond and can reach 20 amps. VFTLP Testing has successfully used 100 ps risetime to produce very useful data for effective CDM protection designs. Small diodes are typically used as protection elements for this threat because they only have to withstand this very short but high current ESD threat. This protection element is also located on chip immediately at its package lead connections. The CDM Discharge from a single lead or ball is determined by the packaged device's capacitance to a nearby ground plane. Low discharge resistance produces a high discharge current, which only lasts for one or two nanoseconds because of the low capacitance. The CDM tester discharges the device capacitance through the tester's

extended pin which makes contact to the device pin or ball. The capacitive discharge through the bond wire and lead inductance added to the inductance of the CDM tester produces a sine wave current waveform. The resonant circuit's relatively high series resistance causes the discharge to be highly damped allowing its rate of rise to be somewhat faster than its rate of fall.

CDM Failures predominately occur in gate insulators, and are caused by the unclamped early part of the ESD voltage. The value of VFTLP is in its ability to accurately measure this voltage threat. As shown in figure 3 the VFTLP test pulse and the CDM current pulse do not have the same waveform. This is because the external discharge current is formed by the LRC elements in the CDM tester. Because currents travel much slower through semiconductors there is a delay between when the ESD voltage is applied to a diode and when it becomes fully conducting. During this time the early part of a rapidly rising ESD voltage is not clamped. Excessive amounts of time delay produce higher unclamped voltages. At some amplitude it will cause the gate insulator to fail.

During the few picoseconds that carriers take to complete the path through the voltage clamping diode, its conductivity is delayed. This allows some part of the early fast rising ESD threat voltage to escape being clamped to a lower acceptable amplitude. Figure 5 below is my graphical analysis of how this occurs.

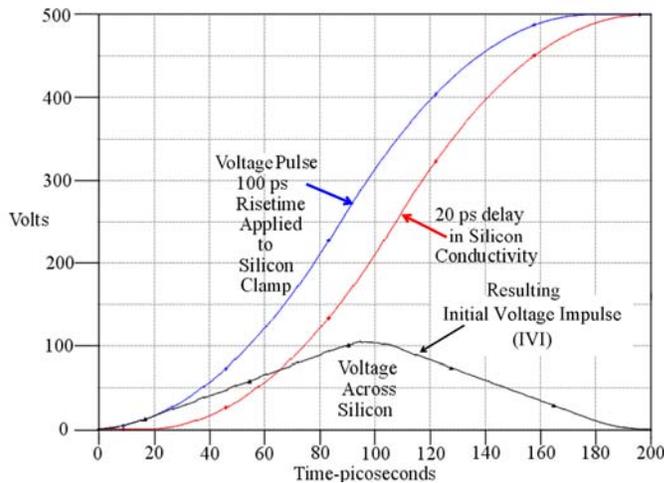


Figure 5. CDM generation of Initial Voltage Impulse (IVI)

The diode is assumed to have a constant 20 ps conductivity delay at all voltages. The increasing voltage applied to the diode initiates more carriers on their path which after their delay achieves increased conductivity. The amount of voltage threat to a gate oxides is the black plot at the bottom which remains unclamped.

VFTLP Operation

The silicon voltage circuit clamp operation is best tested directly on the bare silicon before packaging. VFTLP maintains the high speed properties of 50 ohm transmission lines from the pulse generating switch to two pads connected to silicon voltage clamp element. Testing the clamp circuit without the package's inductive parasitics accurately identifies what occurs inside the package.

The original concept for VFTLP was to provide a short test pulse that simulated the energy dissipation in the CDM clamp similar to that done the TLP test. However because CDM primarily causes oxide failures in core circuits, measuring its cause became much more useful, and silicon failure is only of secondary interest. The rate of voltage rise from external ESD generated by the clamp inside the package cannot be measured outside the package. For the most rapid response, minimum electrical length diodes, and especially gate coupled diodes are used to clamp ESD voltages and protect gate insulators. The primary value of VFTLP is its unique ability to measure the amount of voltage which sneaks by the CDM voltage clamping diode. The following time plot shows a Gaussian ESD 100 ps risetime threat voltage applied to an ESD protection diode.

The typical triangular IVI waveform shown in Figure 6 is measured on CDM protection circuits with a very fast voltage monitor. The triangular shape and width were theoretically derived in reference 2.

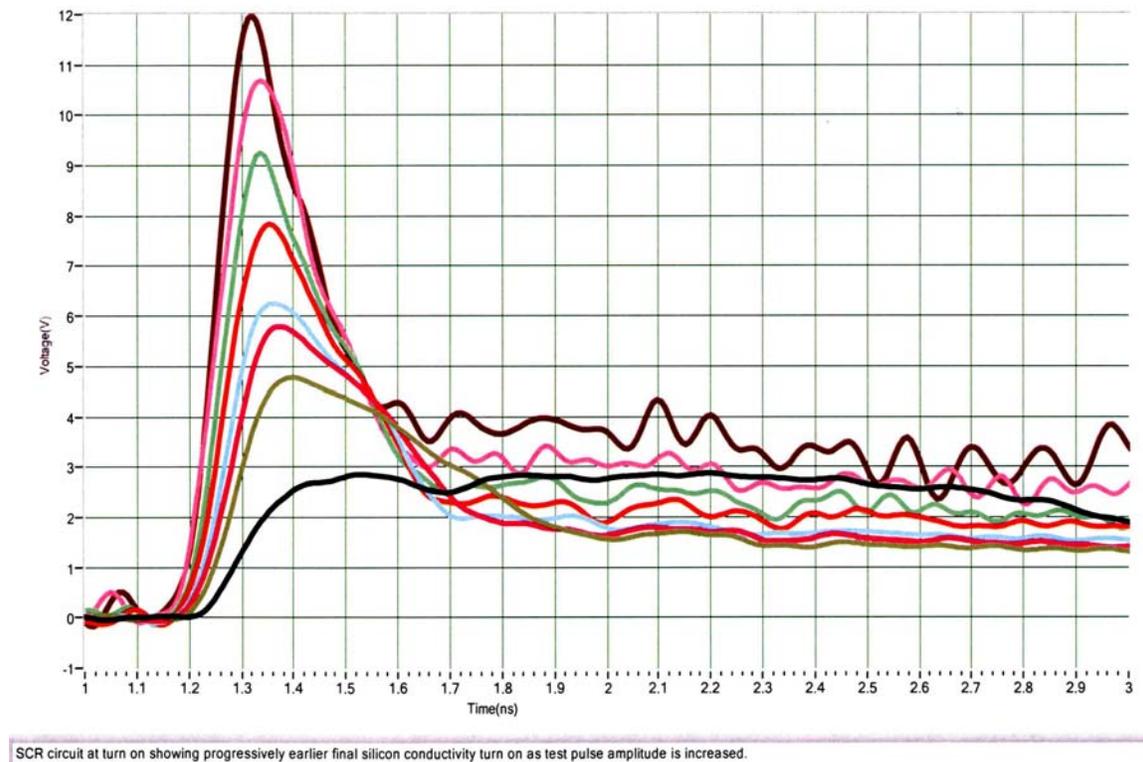


Figure 6. The Initial Voltage Impulse (IVI) waveforms during VFTLP testing

The measured IVI of this a small SCR ESD protection circuit ESD protection circuit started at a low amplitude shown as the lower black waveform. The initial impulse gradually increased in amplitude as the test pulse amplitude and DUT current increased. The triangular IVI waveforms in figure 5 are seen in each protection clamp tested with VFTLP.

A gate monitor should be included with each new CDM protection circuit design and tested with VFTLP. Its failure will be indicated by a leakage current increase which identifies its precise TDDB sensitivity for this short voltage threat. The peak IVI

amplitude is added to the VFTLP I-V characteristics to identify the test pulse current amplitude where each type of gate oxide will fail. [3]

Many types of ESD threats vary in time of rise and duration. [3] Test pulses are generated with special waveform shaping pulse sources to simulate the important rate of rise and/or energy threat which cause the predominate failure mechanism.

Industry Council

The Industry Council was formed in 2006 to provide guidance in general ESD issues for the semiconductor industry and users. Our deliberations have produced four white papers with wide reaching practical advice for the industry and users of semiconductors. All semiconductor manufacturers and many interested user have been invited into the decision making process to make it as thorough and inclusive as possible. Our first responsibility was to establish target levels for HBM and CDM testing as devices became smaller and faster and ESD control methods improved. Reductions in transistor size and operating voltage have made them more sensitive to ESD while improvements in controlling electrostatic charge levels have reduced ESD threats. These white papers [4] on many ESD issues provide a valuable industry consensus useful in understanding this complex new and evolving technology.

References:

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