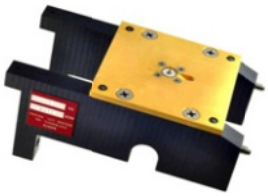
"The Measurement Guys"

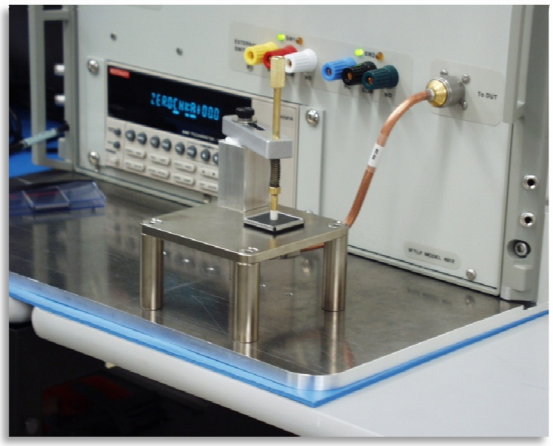
Barth Electronics, Inc.™

ESD Test Systems Catalog

Since 1964

ESD Test Systems
&
Instrumentation





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Barth Electronics, Inc.

ESD Test Systems Catalog ©1/17/23

ESD MODEL NUMBER NUMERICAL INDEX

Barth Electronics, Inc.™

Company Background - ESD Division

Barth Electronics, Inc. is a high technology company specializing in designing and manufacturing “state of the art” sub-nanosecond high energy, pulse power instrumentation since 1964. Originally moving from Ohio to Boulder City, Nevada in 1976 during the days of weapons testing at the Nevada Test Site, we designed and manufactured very special test hardware for EG&G in Las Vegas as well as the National Laboratories. In 1997, Barth test equipment engineers developed the first commercial Transmission Line Pulser (TLP) for the Electrostatic Discharge (ESD) industry, using unique technology developed for high speed, high voltage test equipment.

As the operating transistors inside IC’s have become smaller and more sensitive to ESD, each pin on every IC is now protected to provide the reliability demanded in the digital world. By beating our swords into plowshares, weapons testing hardware was changed into the development and manufacture of the highest quality ESD test equipment available today. The reliability demanded in weapons testing was also transferred into our commercial ESD test equipment. High reliability test equipment is needed to design and test semiconductors to ensure their high reliability. Accurate and dependable TLP testing is vital to identifying electrical characteristics of silicon IC’s.

We are continuously investigating new technologies that can be applied to ESD and are designing new products as the need becomes apparent. Barth Electronics offers a complete line of ESD test systems as well as device testing as a service. We have always offered an UNCONDITIONAL guarantee on every product we sell. We provide solutions to the ever growing needs of the ESD industry.

Barth Electronics, Inc. - Setting the Standard in High Speed ESD Testing!

TECHNICAL SPECIFICATIONS

TESTING FOR GUARANTEED PERFORMANCE

Components are 100% tested with 1000 pulses at their rated voltage and pulse width. The resistance of all ports is measured before and after HV testing. Each unit passes this test only if its resistance, after HV pulsing, increases less than 0.04%. Any higher increase indicates a breakdown, and that unit is rebuilt and retested. In addition to the DC resistance measurements, each unit is also tested for pulse response and reflection coefficient to be certain they meet our specifications. The pulse amplitude and width capability of a unit listed as 5kV/400ns means that it is guaranteed to withstand 5kV rectangular pulses that are 400ns long. **We recommend that DC resistance tests be performed regularly on all of your resistive attenuators, of any make, as an easy detection of resistor failure.** All of our products are guaranteed to perform to their specifications indefinitely when used within its specifications.

MAXIMUM INPUT LIMITATION

The voltage specification of our products is sometimes limited by the breakdown characteristics of the connectors. The voltage limits we use for our specifications are 4kV for the "N" connector, 6kV for the GR 874 connector and 13kV for the "HN" connector. These limitations are for DC, and provide a safety factor for our pulse length ratings. The "N" connector, for instance, can pass 10kV at short (10ns) pulse widths.

The breakdown limitations of our film resistors are related to pulse energy. A unit that has been tested to withstand 5kV, 400ns FWHM rectangular pulses should be able to withstand 10kV, 75ns FWHM rectangular pulses. While this general "rule of thumb" has been found to be useful in practice, we cannot guarantee higher voltages or pulse widths unless we test the particular unit to your pulse specification.

Some units have been designed and rated to withstand exponentially decaying pulses and are listed with a $1/\varepsilon$ notation. An exponentially decaying pulse with a $1/\varepsilon$ time constant has half the energy of a rectangular pulse, with the same FWHM time. Therefore, our resistive units can withstand exponential pulses that have a time constant twice as long as a rectangular pulse.

Please call if your pulse measurement requirements cannot be met by the standard product specifications.

VOLTAGE COEFFICIENT OF RESISTANCE

The voltage coefficient error of our resistive components is less than 1 % at their rated voltage. It is usually significantly lower than this but we cannot specify it any better because of present measurement limitations. **See our Application Note for further information regarding the importance of Voltage Coefficient in pulse voltage measurement.**

PULSE RISETIME

The 10%-90% risetime through our attenuators is listed as τ (tau). It is calculated by taking the square root of the difference between the observed risetime squared and the input risetime squared. This would be the risetime out of our attenuator with a perfect (zero risetime) input. Our risetime and reflection coefficient **measurements are made with a 54120A HP digital sampling system that can be normalized to as fast as 10ps.**

ATTENUATORS ENERGY RATINGS

Attenuator Model	Pulse Energy Rating	
BEI 2	1 mJ	Tight resistance tolerance low voltage MW attenuator
BEI 141	10 mJ	Medium voltage 3 GHz bandwidth
BEI 142	50 mJ	Higher voltage and >12 GHz bandwidth
BEI 102	50 mJ	Higher voltage and 7 GHz bandwidth
BEI 202	200 mJ	Maximum N connector voltage 17 GHz bandwidth
BEI 2237A	800 mJ	HN connector 7 GHz bandwidth
BEI 2239A	2050 mJ	HN connector 3.5 GHz bandwidth
BEI 2536	400 mJ	HN connector, 200 watt average power

VOLTAGE COEFFICIENT OF RESISTANCE

Application Note #1

The purpose of this application note is to describe some important considerations in high voltage pulse measurements with resistors as dividing elements. The term **"Voltage Coefficient of Resistance**" has been around for a long time[1P]; but is seldom used or well understood. As high voltage pulse measurements improve, and higher accuracy becomes available, voltage coefficient errors that could once be ignored now must be considered.

It is well known that the resistance increases with temperature rise of nearly all resistors, including the commonly encountered carbon composition resistor. The temperature **coefficient of resistance** (of a resistor) may be expressed as the ratio of the resistance change to the temperature rise. Such a temperature coefficient classification is useful if the resistance changes uniformly with temperature rise and fall.

Resistors undergo temperature variations not only due to changes in ambient temperature, but also due to dissipation of electrical energy when current is passed through them. It is desirable in measurements using resistors, that their temperature coefficient be small to minimize errors. One can see, for example, that when a measurement apparatus involving resistors is calibrated at low signal levels, the calibration may be invalid at higher signal levels if the resistance values change.

It has also been known for a long time[1] that the resistance of a resistor can change due to a change in the voltage applied to it, even though the temperature may be held constant. The **voltage coefficient of resistance** may be expressed as the ratio of the resistance change in ohms to the corresponding increase in applied voltage in volts when the temperature is held constant. Such voltage coefficient of resistance definition is useful to characterize the resistance change with an increase in applied voltage. Of course, for any useful resistor material, the resistance returns to its original value when the applied voltage is removed.

When a steady voltage is applied to a resistor, it normally undergoes resistance changes due to both applied voltage and temperature increase. The temperature increase is caused by the dissipation of electrical energy in the resistor due to current flow. At low voltages the temperature coefficient is usually larger than the voltage coefficient. This change in resistance is almost entirely due to a temperature change in the resistor.

When a short pulse is applied to a resistor, and very little average power is dissipated in the resistor, its temperature will not rise appreciably. Most of the resistance change of a low temperature coefficient resistor will be due mainly to the application of voltage, and limited to the time when the voltage is applied. When high voltage pulses are applied to low value resistors, the change in resistance can be appreciable, and can be very important in measurement applications.

Measurement of short high voltage pulses are made in investigations of the effects of lightning strikes, EMP testing on electrical equipment, instrumenting underground nuclear tests, and the pulse power industry.

Most resistors have a negative voltage coefficient, which means that at higher voltages, the resistance decreases during the pulse. If the resistance increases with voltage, the resistor has a positive voltage coefficient. This voltage dependent change of resistance happens instantaneously and can be observed to occur in less than 1 nanosecond. If the period of voltage application is too long, the temperature may rise and cause large resistance changes that can mask voltage coefficient effects.

Short pulses applied to many resistors will show voltage coefficient effects during the time the voltage is applied. Although a resistor may not burn out during extensive pulsing, or have a permanent resistance change, it can have significant voltage coefficient changes during the time of the pulse.

The voltage coefficient varies with different resistive materials, and seems to be greatest for materials that are composed of a granular conglomeration of resistive material held together with an insulating binder. Carbon composition and cermet film resistors use these types of resistive materials.

Nonlinear resistivity can easily be displayed by placing a small amount of finely powdered conducting or semiconducting material between two skewed small diameter wires. Graphite, shaved from a pencil or from a carbon composition resistor displays this effect nicely. The effect can be observed using as little as 1 volt between the two wires. The nonlinear voltage versus current ratio can easily be seen on a simple transistor/ diode curve tracer as a nonlinear slope. This nonlinear resistance occurs for both positive and negative voltages and is symmetrical if there is no rectifying contact. Of course, resistors of a few thousandths of an inch in length are not used in high voltage applications; but if you put 1,000 of these small resistors mentioned above, that are three thousandths of an inch long, in series, you would have a resistor three inches long. This resistor, assembled from many low voltage nonlinear junctions, would have a nonlinear resistance when used at 1,000 volts.

The voltage coefficient of resistance of the resistor depends not only upon the length of the resistor, but also upon the conductive interfaces between the resistive particles that make up the resistor. These interfaces result in emission current (tunneling) across microscopic gaps between conductive particles such as graphite. It is complicated by many factors such as size of particles, their size distribution, and electron emission coefficients. If resistance can be obtained without resorting to high resistance contacts between granular low resistivity materials, then low voltage coefficients can be achieved.

Bulk metal resistors have almost unmeasurable voltage coefficients. However, due to the low resistivity of metals, wire wound resistors must be used to achieve reasonable resistance values. The combined inductance and capacitance effects of wire wound resistors prevent their use either at high frequencies or with fast pulses.

Thin metal film can also be used to achieve reasonable resistance values, but these resistors have a high voltage coefficient. This may result from the extremely thin metal film deposited on a very rough ceramic substrate, that allows tunneling or current flow across the ceramic valleys.

Carbon composition resistors are made with powdered or granular graphite material, which has a relatively low bulk resistivity.

VOLTAGE COEFFICIENT OF RESISTANCE

Application Note #1

Many different resistivity compositions are made to cover the 10 ohm to 10 megohm resistor range. The graphite/insulator compositions are held in place with a phenolic binder that also anchors the wire terminals into the carbon resistance element. This is the original construction method for carbon composition resistors and creates a robust and inexpensive resistor.

Ordinary carbon composition resistors normally are made in 1/4, 1/2, 1, and 2 watt sizes. Our measurements found the 2 watt size to have a much higher voltage coefficient than the 1 watt size, and the 1/2 watt size to have the lowest voltage coefficient over all. It was also found that the voltage coefficient of any particular wattage rating is not much different between manufacturers. This would lead us to believe that something in the basic manufacturing process of this type of resistor may be responsible for its very high voltage coefficient.

In order to increase the surface area of a carbon composition resistor and allow it to dissipate more energy, the size of the resistor is increased. Increasing the size of the resistor will usually decrease its resistance unless one increases the resistivity of the bulk material to compensate for the increase in cross sectional area. For example a typical 1/2 watt resistor,P[2 P]has a length of 0.375 inch and a diameter of 0.140 inch. The typical 2 watt resistor has a length of 0.688 inch and a diameter of 0.318 inch. The length has been increased by a factor of 1.8, and the diameter by a factor of 2.27, so that the cross sectional area has increased by a factor of 5.2. The resistance of a cylindrical resistor would be R = r I/A, where r is the resistivity of the bulk material, I is the length, and A is the cross sectional area. The resistance would be increased by a factor of 1.8 due to the longer length, and decreased by a factor of 5.2 due to the larger cross sectional area. This example assumes parallel end terminals, although commercial carbon composition resistors have very non-uniform end terminals.

In order to maintain the same resistance, in going from 1/2 watt size to the 2 watt size, the resistivity of the bulk material must be increased by a factor of 2.9. The resistivity depends upon the ratio of graphite particles (and their size distribution) to the insulating binder material. A higher resistivity is achieved by decreasing this ratio, using more binder or less graphite in the mixture. Therefore, the resistance material of a 2 watt resistor has a smaller percentage of graphite, than a 1/2 watt resistor with the same value. Fewer contacts between granular resistor particles results in more tunneling, causing a higher voltage coefficient.

The mechanism that causes resistors to change value with the application of voltage is difficult to define with certainty. However, the evidence for such a change is real, and substantial changes in resistance can be observed. In one of our tests, the resistance of a 2 watt carbon composition resistor was observed to decrease from 390 ohms to 200 ohms during pulse testing. The high voltage resistance was approximately 51% of the resistance at low voltage during application of a 2kv, 100ns wide pulse. In pulse tests at 3kV with the same value resistors, a 1 watt resistor decreased approximately 15%, and a 1/2 watt resistor decreased approximately 6%.*

An additional factor that probably contributes to a decrease in resistance upon the application of high voltage is the effect of the swaged tinned metal contacts of these resistors. They protrude into the bulk resistive material in such a way as to cause non-uniform current distribution at both ends of the resistor.

In high voltage pulse testing, inaccurate results are obtained when high voltage coefficient resistors are used for voltage division or attenuation measurements. The measurement of voltage coefficient of resistance can be accomplished at audio and radio frequencies by measuring the production of harmonic signals due to resistor nonlinear behaviorP[3P]. We have developed additional measurement methods using voltage pulses, and will continue resistor and attenuator testing.

We hope this information helps provide a better understanding of voltage coefficient and the causes of resistance changes at high voltage. Reduced accuracy is the result of using common resistors in high voltage pulse measurements. The effect of voltage coefficient and the importance of using resistors with a low voltage coefficient in high voltage measurements is gradually becoming more widely appreciated.

Because future designs are based on voltage measurements made today, it becomes obvious that the use of low voltage coefficient resistive instrumentation is essential for tomorrow's designs.

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*This agrees within the limit of 0.02 percent per volt quoted by G.W.A. DummerP[4P]. The results quoted for 1 megohm resistors of 1/4 to 2 watt ratings by F. LangfordSmithsP[5P] cannot be compared to those obtained at Barth Electronics, Inc., because there is no information on the dimensions of the resistors, and because Barth Electronics test resistors had lower resistance values.

REFERENCES

[1] "Measurements of Nonlinearity in Cracked Carbon Resistors", G.H. Millard, Proc. l.E.E. (London) Vol.106B, Jan. 1959, pp.31-34.

[2] "Electronic Designers Handbook", L.J. Giacoletto, Editor, Second Edition, McGraw-Hill Book Co. 1977, pp.3-B.

[3] "Harmonic Testing Pinpoints Passive Component Flaws", V. Peterson and P. Harris, Electronics, July 11,1966, pp. 93-100.

[4] "Materials for Conductive and Resistive Functions", G.W.A. Dummer, Hayden Book Co., 1970, p.279.

[5] "Radiotron Designer's Handbook", F. Langford Smith, Editor, Fourth Edition, Electron Tube Div. RCA, 1953, p.188.

Information on HN and Barth HNB Connectors:

The Barth HNB connector was specifically designed to provide both high voltage pulse capability and fast rise time performance in an HN compatible connector. These two characteristics are not available, both together in any other commercially available HN connector.

While the HN connector interface is not quite as good as the precision N connector, it is still a very respectable connector and has the advantage of withstanding much higher voltages. The HN connector to connector interface will handle 15kV DC at sea level and somewhat higher pulse voltages.

However all HN connector to cable interfaces are not created equal, some are capable of handling high voltages and others are not! The high voltage limitations of a cable connector, or any connector for that matter, are often limited by the transitions on the end of the connector opposite the connector to connector interface. This is especially true of cable connectors, where the center conductor to outer conductor air gap spacing at the cable to connector transition is often not designed for high voltage, that is, it is shorter than the connector interface air gap spacing. A real danger in this is that breakdown can be occurring inside a connector and it will most likely not be apparent at the connector interface.

The Amphenol UG-59B/U male HN cable connectors as well as the Barth 401-HNB male HN cable connectors have a cable to connector interface (center conductor to outer conductor) air path which is 50% longer than the HN to HN interface air path, and thus gives these connectors good high voltage capability. The easiest, and typical design,(as used in the Amphenol UG-59B), to make an HN cable connector handle high voltage is to cut the cable insulation off square and then have the connector insulator overlap the cable insulation by a length which is longer (commonly 50%) than the connector to connector interface air gap path. While this does a good job of providing high voltage capability, it causes a severe discontinuity which limits the bandwidth of this connection.

The Barth 401-HNB male HN cable connector is designed to handle high voltage and provide the best possible bandwidth. The way we provide both high voltage capability and wide bandwidth is to cut down the diameter of the insulation, in the cable to connector interface area, with a special hand tool. The connector insulator will then overlap this area to provide the high voltage capability, and it is made the correct diameter to also provide the correct impedance, which eliminates the discontinuity and therefore the bandwidth limitations inherent of the typical dielectric overlap used in the typical high voltage HN connectors.

Other HN Connectors such as the Kings KH-59-19 male HN cable have an improved RF specification. This improved bandwidth typically is the result of shortening of the dielectric overlap area, and thus creates a reduction in the length of mismatched impedance. This improvement for bandwidth comes at the expense of lower voltage handling capability in the cable to connector interface. In the case of the Kings KH-59-19 male HN cable connector, the cable to connector interface (center conductor to outer conductor) air path is 50% shorter than the HN to HN interface air path, and thus makes this connector unsuitable for high voltage applications. The shorter air gap in the coax to connector interface will almost always break down before break down occurs in the connector interface (where it would be more easily detected).

The Barth HNB interface is completely compatible with the standard HNB interface and when 2 HNB connectors are mated you have the best available match for HN type connectors. If your fast pulse rise times are slower than 0.5ns, you probably wouldn't benefit from the advantages of the Barth HNB connectors, but if your pulse rise times are on the order of 200-300ps then you would see some benefit, and if your rise times are faster than 100ps the HNB connectors are a must.

If your application does not need the wide bandwidth of the HNB connectors, just insure that the HN connectors you are using have a cable to connector interface that will handle your highest pulse voltage pulses.

We hope this information will help you to achieve good test results using HN connectors.

Information on Barth BE 40kV Connectors:

The Barth BE connector is a unisex connector with a mating bullet that was specifically designed to addresses the Pulse Power need for a connector that will take higher voltage than an HN connector, and can still pass fast sub-ns pulse rise times. While the HN connector to connector interface will handle 15kV DC at sea level and somewhat higher pulse voltages. The BE connector to connector interface will handle 40kVDC, at sea level and somewhat higher pulse voltages. The BE connector provides both fast rise time performance, and high voltage pulse capability, for applications up to 40kV. These two characteristics are not both together available in any other commercially available connector at this voltage rating.

Most high voltage connectors are not designed to be wide bandwidth; likewise most RF connectors are not designed to handle high voltage. There are a few RF connectors on the market that will handle 20 to 25kV pulses, and some are matched better than others for rise time performance. Most are limited to a particular cable type, and others are only found on pulse generators and are supplied with the mating connector on a piece of coax.

The high voltage limitations of a coaxial cable connector are often determined by the cable to connector transition, the end of the connector opposite the connector to connector interface. Coaxial cable connectors are typically designed for RF performance, and not with high voltage in mind. Most often the center conductor to outer conductor air gap spacing at the cable to connector transition is not designed for high voltage, that is, it is shorter than the connector interface air gap spacing. A real danger in this is that breakdown can be occurring inside a connector and it will most likely not be apparent at the connector interface.

The coaxial connector, cable to connector interface air path (center conductor to outer conductor), for a well-designed high voltage connector, is made to be longer than the connector to connector interface air path, and thus gives the connectors reliable high voltage capability. The easiest, and typical design to make a cable connector handle high voltage is to cut the cable insulation off square and then have the connector insulator overlap the cable insulation by a length which is longer (commonly 50%) than the connector to connector interface air gap path. While this does a good job of providing high voltage capability, it causes a severe discontinuity which limits the bandwidth of these connectors.

The Barth BE connector is designed to provide the best possible bandwidth and to also reliably handle high voltage. The way we provide both is to cut down the diameter of the cable insulation in the cable to connector interface area with a special hand tool. The connector insulator will then overlap this area to provide the high voltage capability. This allow us to also maintain the correct dielectric diameter to provide the correct impedance, which eliminates the discontinuity and therefore the bandwidth limitations inherent of the typical dielectric overlap design used in most high voltage connectors.

The Barth BE interface is now standard on many of our higher voltage products, and we offer a cable version for RG-214 cable. Other versions will soon be available for RG-217, other high performance low-loss cables, as will be adapters to HN, N, bulkhead feedthroughs and bulkhead flange to transmission line versions. A hermetic feedthrough for vacuum applications is also being planned.

When 2 BE connectors are mated you have the best available match for your high voltage pulse system. If your fast pulse rise times are slower than 1ns, you may not benefit much from the advantages of the Barth BE connectors, but if your pulse rise times are faster than 500ps then you would see some benefit, and if your rise times are faster than 100ps, the BE connectors are a must.

If your application does not need the wide bandwidth of the BE connectors, just insure that the high voltage connectors you are using have a cable to connector interface that will handle your highest pulse voltage pulses. We hope this information will help you to achieve good test results using BE connectors.

What is TLP?

TLP is a short pulse (50ns to 200ns) measurement of the current-voltage (I/V) characteristics of the ESD protection built into an integrated circuit. The short TLP pulses are used to simulate the short ESD pulse threats that the input-output (I/O) pins of an IC must withstand without damage being caused to the complex silicon structures.

The TLP acronym stands for Transmission Line Pulse testing. A constant impedance transmission line is used as a pulse source because it can create a constant amplitude rectangular pulse shape. A flat top rectangular pulse is used because the amplitude at different points along its length can be measured more accurately than can be done with other pulse shapes.

The TLP cable used to generate the rectangular pulse for testing is usually 50 ohm because of the universal availability of coaxial cables and matched coaxial connectors. The coaxial cable is charged with a DC power supply to the desired voltage and then quickly discharged with a low inductance switch. The fastest pulses are made with a switch that is placed in a constant impedance coaxial housing to preserve the fastest possible risetime. A fast pulse can be made into a slower Gaussian risetime by using a matched impedance risetime filter. Such filters slow the pulse risetime without causing any other distortions. This concept is covered more fully in our Application Note #3.

TLP testing is done by applying the rectangular test pulse to the two pins of the Device Under Test (DUT) to be tested. The most common method of introducing the pulse to the DUT has been to split the pulse between a grounded 56-ohm resistor and a 500 to 1500 ohm resistor in series with the DUT pin to be tested. The common pin is connected to the ground lead to provide a return path for the pulse current.

TLP testing typically begins with low voltage pulses that are successively increased in amplitude to provide sufficient points to fill out an I/V plot. Higher or lower amplitude steps can be chosen to provide more or less data points for the areas of interest on the I/V plot. Usually the amplitude of the test pulse is increased until the DUT is damaged to learn its precise pulse current limit. The TLP pulse amplitude increases can be made smaller to add additional test points to some particular area of interest.

Damage to the DUT will occur when the test pulse amplitude becomes high enough to produce enough heat in the DUT to melt some structure and cause a permanent change in the device. Damage is usually accompanied by an immediate increase in the leakage current between the two pins.

A TLP test system includes a leakage measurement after each test pulse as a sensitive monitor of DUT damage. It helps identify precisely which test pulse created sufficient damage to increase the leakage current.

The precise current and voltage amplitudes of the pulse that cause damage to the DUT are then identified by the increased leakage current.

The TLP level of damage information can be compared to HBM damage levels found for the same type of device. TLP testing allows more precise information on damage levels than can be obtained from HBM testing. It allows precise comparisons between different test/production structures as well as providing an I/V plot of the complete electrical operation of the structure throughout its' full range.

The different (I/V) data points are plotted by measuring the pulse current through the device and the voltage across the device near the end of the test pulse. The testing is done near the end of the pulse after the current through the device and voltage across the device have stabilized. Damage to the device will occur near the end of the test pulse that causes enough heating/melting to effect a permanent change. An advantage of TLP testing is to identify the exact test pulse that caused damage to occur.

The temperature, in the silicon structure that absorbs the ESD threat, increases during the rectangular test pulse. The hottest temperatures will be found at the end of the pulse. As the amplitude of each pulse is increased, damage to the device will occur near the end of the test pulse if the step increases in amplitude are made sufficiently small. The goal is to measure the I and V near the end of the pulse to identify the exact pulse where the damage occurred.

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Evaluating a TLP system for purchase decision should be done with a known circuit element. When we developed the *first* commercial TLP system many of our customers tested their devices with TLP trying to evaluate its quality. We recognized the need for an element with known and repeatable electrical characteristics to verify the accuracy of any TLP system. That is why we developed the SOLZ unit. It consists of a short, an open, a load resistor and a few Zener diodes. We measure these repeatable circuit elements to verify their I-V characteristics and provide them to anyone in the industry who wants to verify the accuracy of any TLP system. The short and the open are very simple; but we selected a special Zener diode that has repeatable turn-on sharp knee characteristics. One unit turns on about 7 volts, adding the second one causes turn on to occur at about 14 volts and adding the third Zener diode provides a 21 volt calibration point.

The Zener diodes are calibrated and their individual calibration voltages are provided with each SOLZ unit. We use a SOLZ calibration with each of our TLP systems to insure that the voltage measured is within 2% of the Zener calibrated voltage at three voltage levels.

The L in SOLZ is an accurate value Load resistance element. Measuring it can be used to verify the resistance (I/V) measurement capability of any TLP system. When the I/V data is known and the V data is known (from the Zener diodes) the accuracy of the current measurement can also be identified.

The Barth Model 4002/4003 TLP**+**™ system measures dynamic resistance value, typically, within 3%.

Before you decide on which TLP system to purchase please ask the other TLP manufacturers to measure our SOLZ unit. They can also construct and calibrate the individual elements in their own SOLZ unit.

You cannot evaluate a TLP system based on someone's opinion. It cannot be based on measuring unknown silicon elements that may or may not fail or change with testing. The evaluation of *any* TLP system must be based on measured data of four different known value elements.

If you have any questions on TLP calibration or verification please ask. I have spent many hours with the ESDA working group on TLP explaining and including the use of the SOLZ unit into our standard.

The data is found in ANSI/ESD SP5.5.1-2004 document. Section 7.3 under Tester Verification Methodology explains the methods of its use.

Jon Barth
Chief Engineer

The Barth SOLZ Kit
(For evaluation of TLP test systems)

INSTRUCTIONS FOR USE

The Barth Electronics' SOLZ Kit is used to evaluate the ability of TLP test systems to accurately measure known elements. These elements are a "**Short**", an "**Open**", a "**Load**", and a "**Zener**" diode (hence the acronym **SOLZ**).

The SOLZ Kit is an assembly of six known, measurable elements (including 3 Zener diodes of different voltages) which are stable, repeatable, and affordable. The six elements have been combined into a handy 16 pin DIP package. The six elements, measured by a TLP test system, will reveal basic information about the test system.

Short:
Measuring the short (pins 1 & 16 on the DIP package), will reveal the total internal series resistance of the system (typically ~2 ohms for the Barth Model 4002/4003 TLP test system). Note that the Barth Model 4002/4003 allows the operator to 'compensate' for the series resistance by entering a 'cal value' (see the document "TLP Compensation Procedure" used to calibrate the Model 4002/4003, copy enclosed).

Open:
Measuring the open (pins 2 & 15 on the DIP package), will reveal the total internal shunt resistance (or series conductance) of the system (typically -75 micromhos for the Barth Model 4002/4003 test system). Note that the Barth Model 4002/4003 allows the operator to 'compensate' for the shunt resistance by entering a 'cal value'.

Load (5 ohm resistor):
Measuring the resistor (pins 3 & 14 on the DIP package), will reveal the TLP test system's ability to produce a smooth slope showing a voltage / current ratio of 5 ohms. Five ohms has been chosen to most closely simulate the "on" resistance of a modern protection device. To obtain a full scale slope for the Barth Model 4002/4003, set the pulse voltage scale to 0 to 50 volts, and the current scale to 0 to 10 amps. If the Barth Model 4002/4003 has been 'compensated' by entering 'cal values', the accuracy of the measured resistance is warranted to be within 3%.

Zener (diodes):
Measuring the three Zener diodes' turn-on voltages will reveal the accuracy of **pulse** voltages. Use pin 4 for the negative lead and use pins 13, 12, or 11 for the positive lead (for the 7v, 15v, and 24v Zeners, respectively). To measure system accuracy, compare the TLP systems' measured turn-on voltages with the SOLZ Kits' labeled voltage values (typically 1 to 2% accuracy for the Barth Model 4002/4003 test system). The Barth system accuracy is warranted to be within 3%.

Please contact beisales@barthelectronics.com for further information.

TLP Test System
Barth Model 4003 TLP+ ™

The Barth Model 4003 TLP+ ™

Pulse Curve Tracer precisely characterizes the ESD robustness of silicon chip protection circuitry. Programmed rectangular pulses are applied to the device under test, resulting in a computerized plot of current vs voltage. A leakage measurement can be made after each pulse to obtain the leakage evolution current versus pulse voltage. Set up for packaged device testing; an optional dual wafer probe (Model 45003WP), permits wafer level testing. Other options and accessories are also available.

System Components:

- Tektronix 1 GHz, 2 channel, digitizing oscilloscope
- High reliability Barth Electronics control box/pulse generator
- Keithley Picoammeter/voltage source
- Dell Precision Workstation - Test control computer
- LabView® runtime control and analysis software
- One year warranty on the entire system
- One year BSSP Barth Software Subscription Program

How It Works

Operation of the 4003-TLP Pulsed Curve Tracer is very intuitive. The operator adjusts the desired test parameters via keyboard, such as starting voltage, current and voltage limits, voltage step increments, pulse risetime, leakage test voltage, and pulse width. The operator then selects to start a test and the test proceeds automatically, controlled by Barth software developed with National Instruments Labview©. The operator can halt and resume the testing and can view the plotted test data points as the test proceeds.

The operator can also view (during testing or afterward), voltage & current waveforms, single point or multi-point leakage evolution, test set-up parameters, or numerical data information. The active test and several previous tests' data points may be viewed simultaneously on the I/V plot.

Hardcopy printouts listing data point values and showing plotted results using operator selected scaling are immediately available in a presentation ready format at the end of a test.

Accuracy

Special Barth wide bandwidth pulse current and voltage sensors provide a high standard of measurement capability for ESD test equipment.

The complete system has been built with special attention paid to minimizing losses in the test circuitry and the coaxial cable connections. This results in low internal resistance at the device under test (DUT), for high accuracy measurements.

Barth's software allows users to make manual leakage delay adjustments, and allow for leakage test voltages up to 500V. Higher values are available with optional source meter.

The software includes voltage & current waveform capture, automatic calibration / compensation, automatic data save, save / recall operator set-ups, auto or manual axis scaling, single or multi-point leakage testing (configurable), adjustable measurement window, dynamic resistance calculator, recall data function for compare & analyze of multiple tests, 2 channel scope (4 channel optional), save / recall pulsing "profiles", scope auto-SPC (signal path compensation), and numerous other features.

The BSSP (Barth Software Subscription Program) provides periodic software updates and improvements. This assures your system is in peak operating condition. Test speed increases, and efficiency improves. Improve system capability with regard to calibration, reporting, and system diagnostics; all available with BSSP.

Barth Electronics, Inc.
1589 Foothill Drive
Boulder City, NV 89005
Phone 702.293-1576
Fax 702.293.7024
www.BarthElectronics.com

TLP Test System
Barth Model 4003 TLP+ ™

Specifications:

- Pulse current: 30 amps @ short circuit; 0-10 amps @ 50Ω load, 40A options available
- Pulse width: 75ns to 150ns standard; 500 ns option available
- Standard pulse width of 100ns (and 75ns) is supplied with the tester. Pulse width is manually selectable
- Pulse voltage: 0-500 v @ 50Ω load, 1000 v @ open circuit (step increments: ≥0.05v)
- Pulse risetime: (10-90%): 0.2, 2, 10 ns (built-in, software selectable) optional rise time filter values are available
- Pulse rate: Up to 20 test pulses per minute
- Leakage voltage: 0 to +/-500v (Model 6487), +/-200v (Model 2400),
- Leakage current sensitivity: 10-12 to 2.5 x 10-3 amps (Model 6487)
- Source impedance: 50Ω
- Load Impedance: any load
- Selectable mains power: 100,120 vac@5amps; 220,240 vac@3amps, 50 to 60 Hz (USA default:120 vac; 60 Hz)
- Switching control for 2 external channels is standard; switching control allows bias voltages to be applied or removed during the leakage test.

Features and Benefits

50 Ohm Test System

Controlled 50-ohm impedance throughout the complete measurement chain of the test system minimizes the measurement errors associated with the usual 500-ohm resistor connections for ordinary TLP testers. Making measurements at 50-ohm impedance minimizes the effects of parasitics.

Just as the Barth 4003 TLP Pulse Curve Tracer connections to the packaged device sockets are constructed with a controlled 50-ohm impedance, the Barth TLP wafer probe also has a controlled 50-ohm impedance throughout its connections to the two needle contacts at any two pads.

Testing the DUT directly from an, inherently low 50-ohm source impedance provides inherently higher pulse currents from a clean test pulse with no ringing or overshoot. A perfect sub nanosecond risetime pulse generator combined with low distortion measurement probes and controlled impedance connections allows the Barth Pulse Curve Tracer test system to gather accurate TLP data either on wafer or on packages.

Data Output

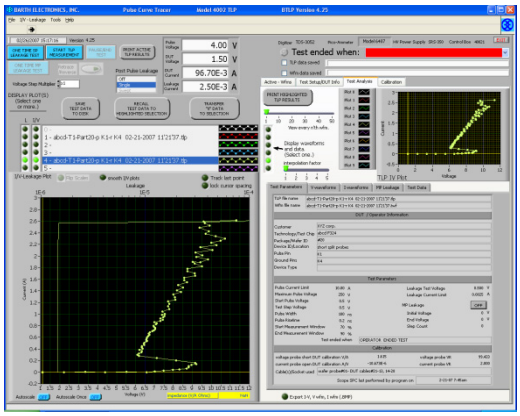
Hardcopy color printouts can be quickly printed that list data point values and show plotted results using operator selected scaling. The numerous software options provide for output of test data, including subsets and comparison printouts containing several tests. User control of scaling and ability to turn on and off leakage data individually for each data set allows the operator to quickly focus in on the important data.

Screen Displays

One of the 8 display screens is shown below.

All 8 screens display the active I-V test data and data for up to 5 recalled tests (on the left half of the screen).

The left side display shows both the I/V curve and leakage evolution. The right side display can also show: V & I waveforms, single or multi-point leakage evolution, operator info, test parameters, numerical test-point data, or calibration values.



Data Storage

Both I-V and waveform data Data is automatically stored to hard disk in tab delimited format and can be recalled for viewing or transferring to disk. Data is automatically time/date stamped when saved.

Size and Weight

System is approximately 19” x 19” x 19” w/scope.
Total weight including Control Box and scope is approximately 75 lbs. (Weight does not include computer.)

- Options and Accessories are available.

This Product Features Barth Designed ZAPLESS ® High Speed Measurement Components

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TLP Test System Options For Barth Model 4003 TLP+ ™

Barth Model 4003 TLP+™

- The Pulse Curve Tracer precisely characterizes the ESD robustness of silicon chip protection circuitry.
- Programmed rectangular pulses are applied to the device under test, resulting in a computerized plot of current vs. voltage.
- A leakage measurement can be made after each pulse to obtain the leakage evolution current versus pulse voltage.
- Set up for packaged device testing; an optional dual wafer probe permits wafer level testing

100ns pulse width - TLP External Charge Line Option Model - 46001-100
125ns pulse width - TLP External Charge Line Option Model - 46001-125
150ns pulse width - TLP External Charge Line Option Model - 46001-150

500ns Wide Pulse Option – Model 4003-02
The Wide Pulse Option extending capability is up to 500ns pulse width and provides one (1) External Charge Line (length of your choice). Note: the control box will need to be returned to factory for modification.

175ns pulse width - TLP External Charge Line Option Model - 46001-175
200ns pulse width - TLP External Charge Line Option Model - 46001-200
250ns pulse width - TLP External Charge Line Option Model - 46001-250
400ns pulse width - TLP External Charge Line Option Model - 46001-400
500ns pulse width - TLP External Charge Line Option Model - 46001-500

40 Amp Option Bundle – Model 4003-15
The 40A Option Bundle provides “True 40 Amp” pulse capability and includes 2,000 volts to an open and 40 Amps through a short. Note: the control box will need to be returned to Barth for modification.

- This option also allows user to analyze HBM and/or HMM circuits for operation characteristics and immunity.

Pulsed Bias Option – Model 4003-07
The Pulsed Bias Option is AC Powered and provides an automatic bypass connection to preserve the leakage test capacity that occurs between TLP stress pulses. Note: the control box will need to be returned to factory for modification.

1500ns Wide Pulse Option – Model 4003-08
Requires 500ns Wide Pulse Option (Model 4003-02); extends capability up to 1500ns wide pulses; Includes (1) 1000ns Charge Line (Model 46001-1075) that is used with the external 500ns (425ns actual) Charge Line (Model 46001-500) to achieve the 1500ns pulse width.

Keithley Model 2400 Upgrade Option - 4003-11
Replaces the Keithley 6487 Model.

580-NFT
80 ns Ramp Generator. Call our office for details.

Computer Upgrade BCCU-4003 (Replacement Computer for Existing Systems)

The Computer Upgrade Bundle includes a Dell Precision Work Station, 19” Monitor, WIN 10, National Instruments Interface Control Board: NI PCIE-GPIB w/NI-488 Software, 3 year Dell Pro Support Warranty on Computer, Software Upgrade, Barth Software Subscription Plan Includes 1 year BSSP

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TLP Test System Options For Barth Model 4002 TLP+ ™

Barth Model 4002 TLP+™

- The Pulse Curve Tracer precisely characterizes the ESD robustness of silicon chip protection circuitry.
- Programmed rectangular pulses are applied to the device under test, resulting in a computerized plot of current vs. voltage.
- A leakage measurement can be made after each pulse to obtain the leakage evolution current versus pulse voltage.
- Set up for packaged device testing; an optional dual wafer probe permits wafer level testing

20 Amp Option – Model 4002-01
The 20A Option is "True 20 Amp" pulse capability and provides 1,000 volts to an open and 20 Amps through a short. Note: the control box will need to be returned to factory for modification.

- This option also allows user to analyze HBM and/or HMM circuits for the operation characteristics and immunity.

500ns Wide Pulse Option – Model 4002-02
The Wide Pulse Option is up to 500ns pulse width and provides one (1) External Charge Line (length of your choice). Note: the control box will need to be returned to factory for modification.

1500ns Wide Pulse Option – Model 4002-08
Requires 4002-02 500ns Wide Pulse Option; Includes (1) 1000ns Charge Line that is used with the external 500ns (425ns actual) Charge Line to achieve the 1500ns pulse width. 1500ns Wide Pulse Option is limited to below 10 Amps max.

Negative Pulse Option – Model 4002-03
The Negative Pulse Option adds an inverter to the pulse circuit; this option is easily installed by user.

30 Amp Option Bundle – Model 4002-05
The 30A Option Bundle provides "True 30 Amp" pulse capability and provides 1,500 volts to an open and 30 Amps through a short. Note: the control box will need to be returned to Barth for modification.

- This option also allows user to analyze HBM and/or HMM circuits for operation characteristics and immunity.

Pulsed Bias Box Option – Model 4002-07
The Pulsed Bias Box Option is AC Powered and provides an automatic bypass connection to preserve the leakage test capacity that occurs between TLP stress pulses. This option is user installed.

Keithley Model 2400 Upgrade Option - 4002-11
Replaces the Keithley 6487 Model.

Computer Upgrade (Replacement Computer for Existing Systems)
BCCU-4002
Barth 4002 TLP Computer Upgrade Bundle: Includes a Dell Precision Work Station, 19" Monitor, WIN 10, National Instruments Interface Control Boards: NI PCIE-GPIB w/NI-488 Software, NI DIO control board, DIO Jumper assembly w/custom bracket, 3 year Dell Pro Support Warranty on Computer, Software Upgrade, Barth Software Subscription Plan Includes 1 year BSSP

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TLP Test System Accessories For Barth Model 4002/4003 TLP+ ™

Pulse Curve Tracer Accessories

20ns Risetime Filter – Model 40010-UC
The 20ns risetime filter provides 20ns up to 30 amp system.

30ns Risetime Filter – Model 40010-WC
The 30ns risetime filter provides 30ns up to 30 amp system.

40ns Risetime Filter – Model 40010-VC
The 40ns risetime filter provides 40ns up to 30 amp system.

Aluminum Test Stand – Model 43002
The aluminum test stand is to stabilize DUT cables during use

DUT Cable for Test Stand – Model 43102
Test stand DUT cable (Section 1; 18" length)

DUT Cable, 2 leads – Model 44202
DUT cable with 2 leads, for 48 pin DIP Zip test fixture (Multiple ground pin)

DUT Cable, 3 leads – Model 44203
DUT cable with 3 leads, for 48 pin DIP Zip test fixture (Multiple ground pin)

DUT Cable, 4 leads – Model 44204
DUT cable with 4 leads, for 48 pin DIP Zip test fixture (Multiple ground pin)

HBM Dual Wafer Probe – Model 45003WP
The HBM dual wafer probe includes 2 DUT cables, needles and accessories

HBM Dual Wafer Probe 3rd Arm Assembly – Model 46010
The 3rd arm assembly is for use with the HBM Dual Water Probe, it is a single probe, and includes a leakage box kit.

- Model 47150 = 50 ohm (set of 2), Source Z = 150 ohms
- Model 47250 = 100 ohm (set of 2), Source Z = 250 ohms
- Model 47450 = 200 ohm (set of 2), Source Z = 450 ohms

Needle: Osmium tipped – Typically used for wafer pad probing (can be used with care for BGA)
Model 45121 - Improved strength Osmium tipped needle (.026" dia. shank, 15 degree included angle to tip, 12.7 micron (0.0005") tip radius. Sold in sets of (4).

Needle: Chisel tipped – Typically used for BGA and other package devices (dead bug style)
Model 45104 - Chisel tipped needle (0.026" dia.shank, wide chisel = .026" ≈660 micron tip width)
Model 45106 - Chisel tipped needle (0.026" dia. shank, narrow chisel = .010" ≈254 micron tip width)
Model 45108 - Chisel tipped needle (0.026" dia. shank, very narrow chisel = .006/.008" ≈152-203 micron tip width)

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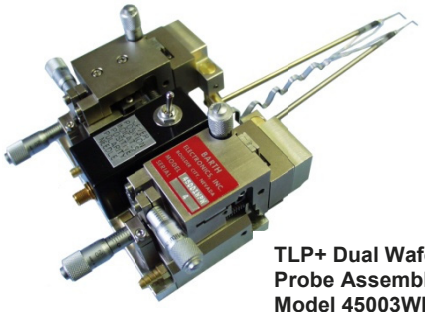
Dual Wafer Probe, 3rd Arm Accessories Barth Model 45003WP, Model 45010

Specifications:

- Dual Wafer Probe High Z Set; each set includes three (3) resistor sets for each Model of High Z.
- Needle: Osmium Tipped - Model 45121
- Needle: Chisel Tipped - Model 45104
- Controlled 50 ohm impedance throughout the complete measurement chain of our test system minimizes the measurement errors associated with the usual 500 ohm resistor connections for ordinary TLP testers. Making measurements at 50 ohm impedance minimizes the effects of parasitics.



TLP+ Dual Wafer Probe Assembly Model 45003WP

The Barth Model 45003WP Dual Wafer Probe accessory is designed to be used with the Barth Model 4003 TLP+ ™ Pulse Curve Tracer for pulse testing of the ESD protection circuit I/V characteristics at the wafer level.

It has two separate needles and isolated probe connections that can be independently positioned with no interaction between them.

Accuracy

The Barth Model 45003WP Dual Wafer Probe accessory has been specially designed to provide the same accuracy as when testing packaged devices in a socket. Testing the TLP characteristics of the device on wafer and later when it is packaged, can provide significantly more information than is available with pass or fail testing with human body model or machine model. Either manner of connecting to the DUT allows very repeatable measurements at high pulse currents.

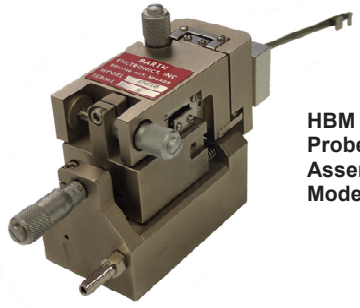
To minimize the mechanical problems of crossed needles in connecting to the pads to be tested, a specially designed constant impedance-reversing switch allows easy selection of the TLP pulse polarity at the pads. A user selectable magnetic or vacuum base allows this TLP probe to be easily moved while maintaining a secure position on the table.

Just as the Barth TLP Test System connections to the packaged device sockets are constructed with a controlled 50 ohm impedance, the Barth Model 45003 Dual Wafer Probe accessory also has a controlled 50 ohm impedance throughout its connections to the two needle contacts at any two pads.

Testing the DUT directly from an inherently low 50 ohm source impedance provides inherently higher pulse currents from a clean test pulse with no ringing or overshoot. A perfect sub nanosecond risetime pulse generator combined with low distortion measurement probes and controlled impedance connection allows the Barth Model 4003 TLP+ ™ Pulse Curve Tracer test system to gather accurate TLP data either on wafer or packages.

3rd Arm Probe Model 45010

The Barth Model 45010 3rd. Arm Probe has been specially designed for applying additional grounds or bias voltages to your devices.



HBM Dual Wafer Probe 3rd Arm Assembly Model 45010

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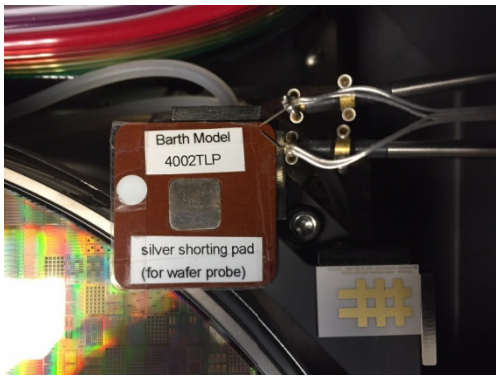
Silver Shorting Pads
Barth Model 45201 and 45202

APPLICATION:

4002-TLP Wafer Probe Short Calibration



Model # 45201

Specifications:

Standard shorting pad supplied with the 4002-TLP and 4003-TLP Test Systems

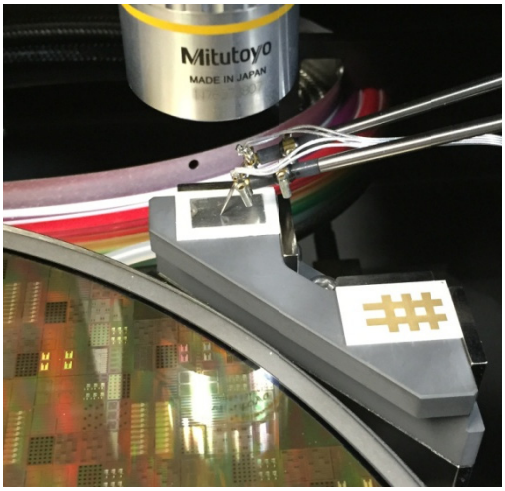
Silver pad located on larger composite back for placement on wafer chuck to provide a calibration short to the Dual wafer probe needles.

Barth Electronics has been the worldwide leader in High Voltage pulse instrumentation since 1964. All of our products are unconditionally guaranteed to perform precisely to our listed specifications. Call or email us for additional information or to discuss your application.

Specifications:

This is an optional shorting pad for use with the 4002-TLP Test System

A Silver pad is located on small alumina base intended for permanent mounting on a probe station frame to allow a short calibration or verification without removal of the DUT wafer from the platen.



Model # 45202

Barth Electronics, Inc.
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www.BarthElectronics.com

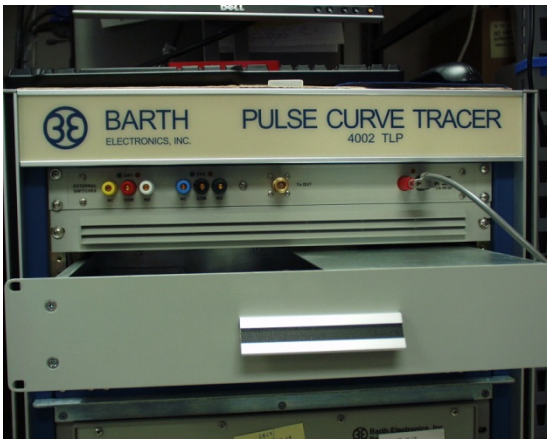
Pulse Bias Box
Barth Model 45320

Option 4002-07
TLP Pulsed Bias Accessory for 4002-TLP

Pulsed Bias accessory for 4002-TLP Pulsed Curve Tracer

APPLICATION:

4002-TLP biasing of the TLP pulsed pin



Unit shown mounted; replaces original "Remote Switches / To DUT" panel on front of 4002-TLP rack chassis.

The Pulsed Bias unit incorporates a wide bandwidth DC blocking capacitor to allow application of bias voltage on the TLP pulsed pin, with built in switching to preserve normal leakage measurement capability; leakage measurements are made in between TLP pulses. Accessory is supplied with a Keysight low voltage power supply which is set up and controlled by the TLP test system over GPIB bus.

Contact us for additional information or to discuss your application.

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Ramp Module
Barth Model 580-NFT

40ns and 80ns Ramp Pulse For 4002

Linear Ramp accessory for 4002-TLP Pulsed Curve Tracer

APPLICATION:

4002-TLP Pulsed Curve Tracer – Ramp Generator (rise time spoiler)

Unit shown mounted; tucks inside top rear of 4002-TLP rack chassis at top of rack inside rear compartment door

Unit connects to the external rise time spoiler connections on the 4002-TLP to provide both 40 and 80ns rise time linear ramp function to the TLP test system.

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Contact us for additional information or to discuss your application.

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TLP Test System Rent (Lease Options)
Barth Model 4002/4003 TLP+ ™

The Barth Electronics Model 4002/4003 TLP+ ™ test system is a complete turnkey TLP test system featuring a Barth Model 40021 TLP Control Box or 40031 TLP Control Box, which includes built in software selectable rise time filters for pulse rise time values of 200ps, 2ns, and 10ns.

Unless otherwise requested, rental unit is shipped configured for the TLP standard 100ns pulse width, and can be easily re-configured by the user for a 75ns pulse width. A control computer is also provided.

Additionally, Barth offers a Model 4002/4003 rent-to-own program. Please contact our office for further details.

System Components:

- Tektronix 500 MHz, 2 channel, digitizing oscilloscope
- High reliability Barth Electronics control box/pulse generator
- Keithley Picoammeter/voltage source
- Main power switch/power distribution panel
- Test control computer
- LabView® runtime control and analysis software

Rental system includes:

- 1 day training on site at the Barth Electronics factory in Boulder City, NV; (travel costs are not included),
- Additional training days are available
- Phone and email support
- Portable TLP+ system which includes:
  - Tektronix® oscilloscope (2 channel)
  - Keithley Picoammeter
  - SRS HV power supply
  - LabView® runtime control and analysis software
  - Control computer with the latest version of Barth test computer software
  - 48 pin DIP zip test fixture (includes DUT cable and accessories)

Currently, systems are only available for rent within the USA.

System availability is limited and subject to prior rental.

Available True 30 Amp System:

- The 30 amp system has “True 30 Amp” pulse capability and provides 1,500 volts to an open and 30 amps through a short. This option also allows user to analyze HBM and/or HMM circuits for operation characteristics and immunity.

This Product Features
Barth Designed ZAPLESS ®
High Speed Measurement Components

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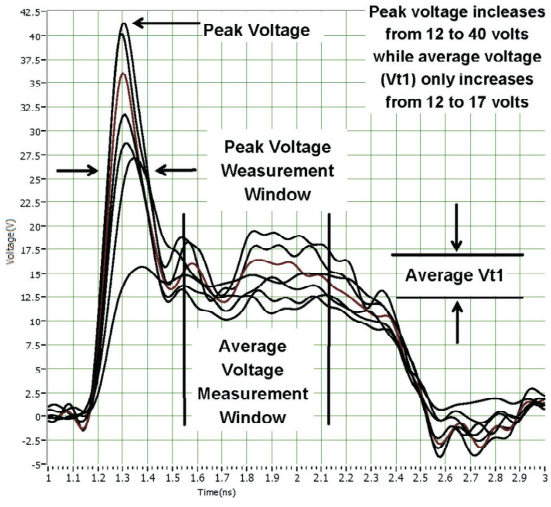
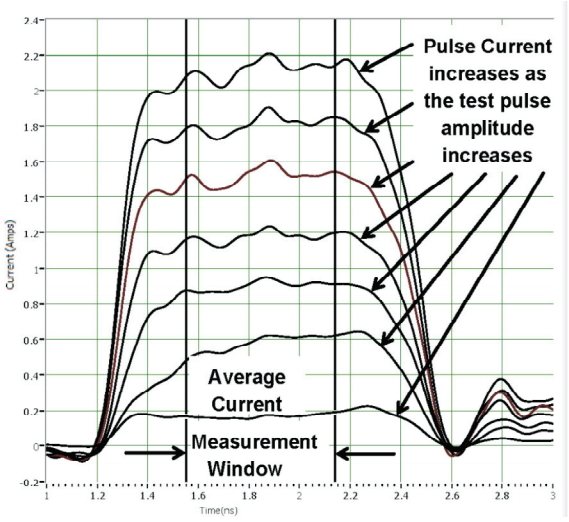
Measure your CDM protection with VFTLP+

Would you like to see the subnanosecond operations of your CDM protection?

VFTLP+ now provides revolutionary improvement in understanding CDM effects inside the package. This test is now available to help you analyze your CDM circuit design. Very Fast test pulse and Measurements simulate the very fast CDM event. Understand the very fast operation of your voltage clamping circuits for the first time.

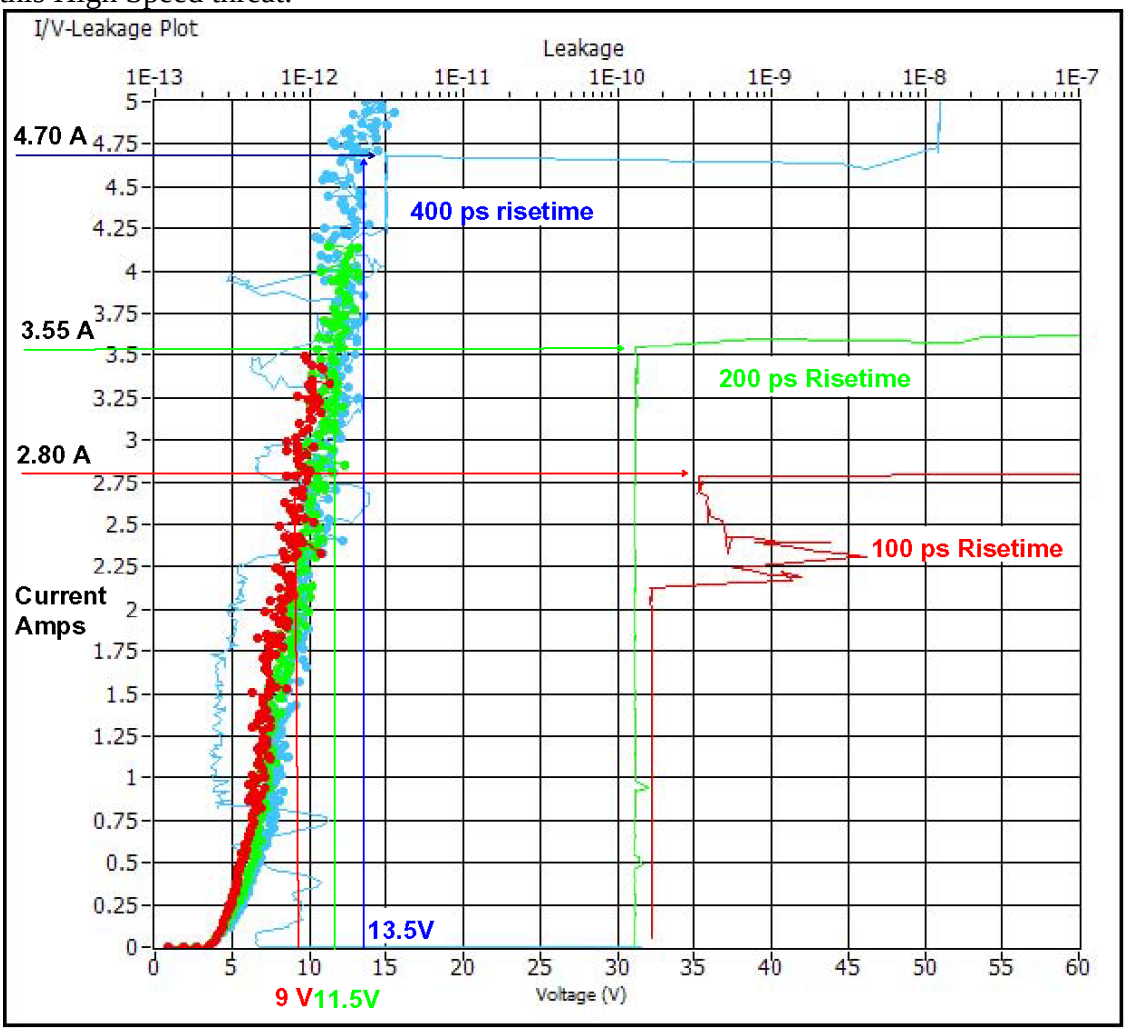




The voltage and current waveforms shown above are of a snapback device. The Voltage waveforms show the Vt1 voltage increasing from 12V to 17V while the peak voltage added threat to the Gate Oxide increases from 12 to 40 Volts. Measurements on wafer; and of packaged devices provides a completely new understanding of CDM circuit operation inside the package.

Barth Plots the "Real" CDM Killer of Gate Oxides

Being able to measure and provide the total voltage over time in an ESD test is a significantly new advancement in ESD design. This is especially true for CDM design because voltage kills Gate Oxides. Modern oxides are thinner and have greater sensitivity to over-voltage. The extremely short but very high voltage requires a new test to measure this High Speed threat.



This above plot shows the ordinary I-V plot of a protection circuit which begins conduction at 4 volts and reaches 10 or 15 volts at currents where the gate oxide fails. The ordinary I-V data averaged during the measurement window at late time doesn't provide the data needed. Current, is not what damages gate oxides however; the short impulse of voltage is the real threat.

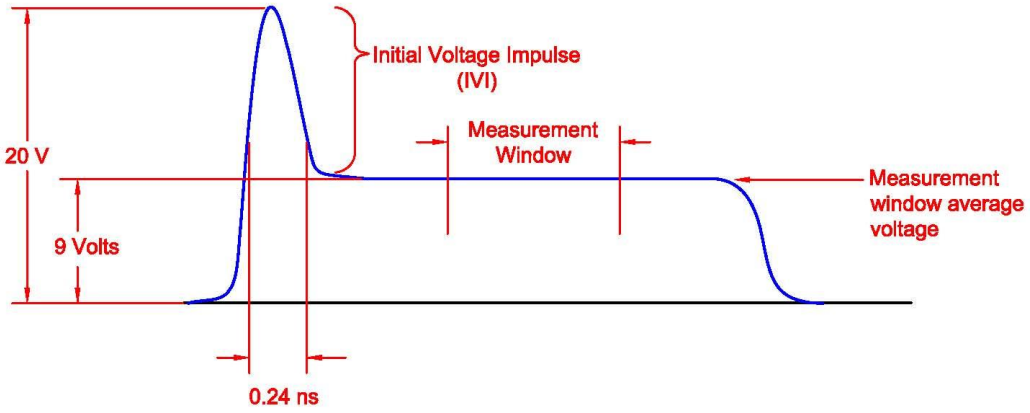
Until recently the true parameters of the very fast voltage waveform threat to gate oxides was unavailable. Because CDM can be as fast as 100 ps risetime, this very fast risetime must be available to simulate the real CDM event. Sensors to measure any rate of rise must be at least three (3) times as fast as the risetime being measured. Barth Electronics has recently developed sub-nanosecond sensors which allow accurate measurements of both the very fast risetime current and voltage in CDM protection circuits.

Barth Plots the "Real" CDM Killer of Gate Oxides

Sensors to measure any rate of rise must be at least three (3) times as fast as the risetime being measured. Barth Electronics has recently developed 30 ps risetime capable voltage and current sensors to provide accurate measurements of the very fast risetimes inherent in CDM protection circuits.

We capture all High Speed data in the current and voltage waveform. The very fast voltage which results from that current pulse is the important parameter needed for CDM protection design. Without 30 ps risetime sensor response, the true voltage threat information necessary for CDM design is not available. The Barth Model 4012 now uses 30 ps risetime I & V sensors to provide accurate measurements of 100 ps risetime pulse used to simulate the CDM event threat.

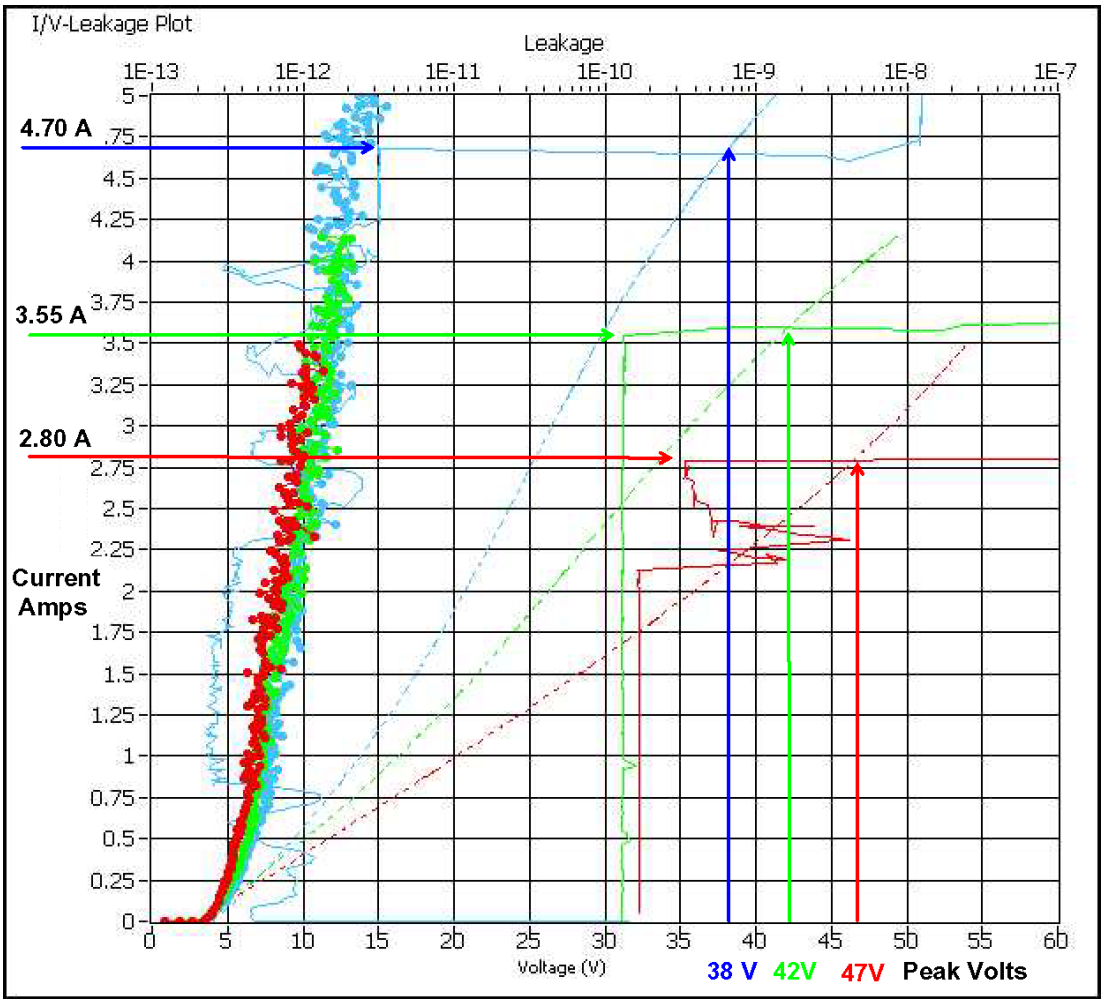
The drawing below shows a typical DUT voltage waveform on wafer which ultimately damages the gate oxide.



Initial Voltage Impulse threat to Gate Oxides
Caused by delay in semiconductor conductivity

The average voltage in the measurement window occurs long after the all important initial impulse voltage. The peak voltage amplitude and its width can now be accurately measured with the High Speed Barth Model 4012 VFTLP+ system. It can measure the sub-nanosecond voltage impulse threat to gate oxides.

Barth Plots the “Real” CDM Killer of Gate Oxides



The above I-V plot made with the Barth Model 4012 VFTLP+ shows not only the voltage averaged during the measurement window, it shows the much higher peak voltage that is the primary threat to gate oxides. The much higher initial peak voltage is a much greater threat than the average voltage measured after the semiconductor has fully turned on.

The Barth Model 4012 system is the only VFTLP+ with extremely fast sensors which can measure this extremely short voltage and identify the dangerous sub-nanosecond peak amplitude. From the sub-nanosecond to many nanoseconds, the 4012 system is fast enough to show both the amplitude and width of over-voltage threats to gate oxides. Gate oxides can be killed by voltages too fast and too short to be accurately seen by ordinary VFTLP systems. Can your VFTLP system show the true data that is this fast?

Does your designer have enough time to design CDM with a VFTLP system which isn’t fast enough to show the Real threats? This VFTLP provides the data you need to determine how your CDM protection responds to the real threat. Real analysis for real first time design, the Barth Model 4012 VFTLP+ can do it!!

VFTLP Test System
Barth Model 4012 VFTLP+ ™

Very Fast High Speed Pulse Curve Tracer

System Components

- Tektronix 6GHz digitizing oscilloscope
- High reliability Barth Electronics control box/pulse generator
- Keithley Picoammeter/voltage source
- Test control computer
- LabView® runtime control and analysis software
- One year warranty on the entire system
- One year BSSP Barth Software Subscription Program

Computer Upgrade
(Replacement Computer for Existing Systems)

BCCU-4012

Includes a Dell Precision Work Station, 19" Monitor, WIN 10, National Instruments Interface Control Board: NI PCIE-GPIB w/NI-488 Software, 3 year Dell Pro Support Warranty on Computer, Software Upgrade, Barth Software Subscription Plan Includes 1 year BSSP

How It Works

To use the Pulse Curve Tracer, the operator enters the desired test parameters via keyboard, such as starting voltage, current and voltage limits, voltage step increments, pulse risetime, and pulse width.

The test then proceeds automatically, controlled by Barth software developed with National Instruments LabView®.

The operator can halt and resume the testing and can view the plotted test data points as the test proceeds.

The operator can also view (during testing or afterward), voltage & current waveforms, single point or multi-point leakage evolution, test set-up parameters, or numerical data information.

The active test and several previous test data plots may be viewed simultaneously on the I/V plot.

Hardcopy prints are immediately available; this includes both the active I/V plot plus leakage vs. average current plot.

Screen Displays

Eight display screens all display the active test and up to 5 recalled tests (on the left half of the screen).

The left side display shows the I/V curve and leakage evolution.

The right side display can also show: V & I waveforms, single or multi-point leakage evolution, operator info, test parameters, numerical test-point data, or calibration values.

The Barth Model 4012 VFTLP+ ™ Very Fast Pulse Curve Tracer is built with specially designed high speed hardware.

Its test pulse simulates the CDM speed and its current and voltage sensors capture the very fast response of ESD circuits necessary for CDM design.

Barth manufactured hardware has the fastest instrumentation of any system and corrects for losses inherent at these picosecond speeds. This system is the first to add accurate peak TDDB oxide threat data to the usual I-V data plot. It is used to analyze the gate oxide threat produced by ESD protection structures. This system captures both voltage and current waveforms at silicon level before packaging for first silicon CDM success.

Software

The software includes voltage & current DUT waveform capture, automatic calibration / compensation (and save / recall), save / recall operator set-ups, auto or manual axis scaling. Single or multi-point leakage testing (configurable), adjustable measurement window, dynamic resistance plots with values, compare & analyze multiple tests, save / recall pulsing "profiles", multi pulsing capability (between data collection points), and scope auto-SPC (signal path compensation), to aid your CDM design effort.

The BSSP (Barth Software Subscription Program) provides periodic software updates and improvements. This assures your system is in peak operating condition. Test speed increases and efficiency improves. Improve system capability with regard to calibration, reporting, and system diagnostics; all available with BSSP.

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VFTLP Test System
Barth Model 4012 VFTLP+ ™

Specifications:

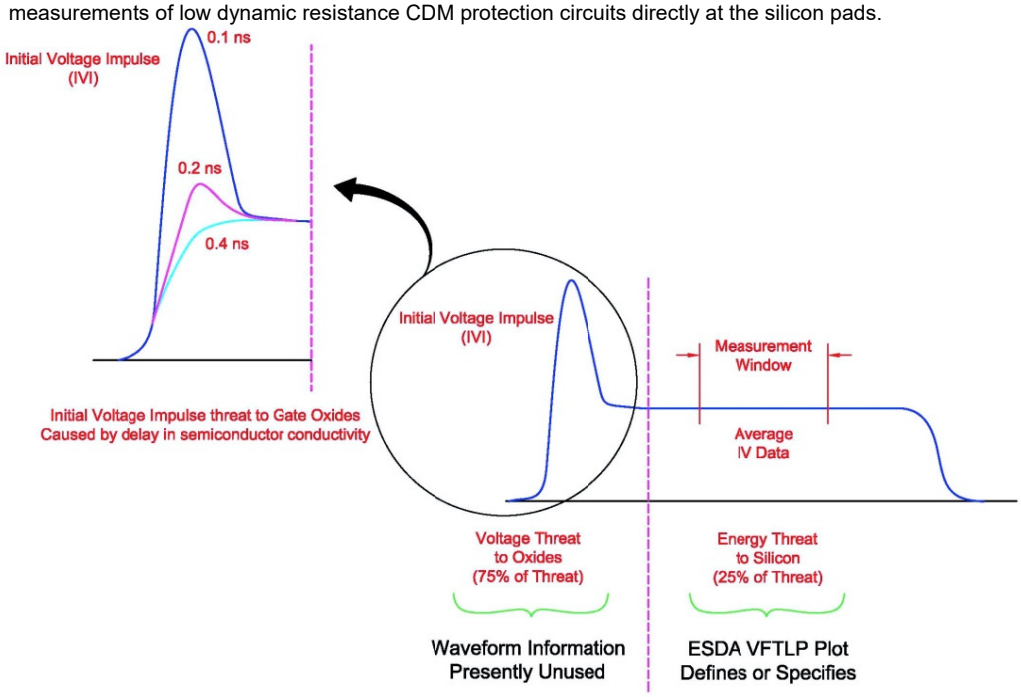
Output to DUT (program driven)

- **Pulse width: 1ns, 2ns, 5ns, and 10ns standard. Pulse width is software selectable.**
- **Pulse voltage: 0-500 v @ 50Ω load, 1,000 v @ open circuit**
- **Min. Pulse Voltage; 1.0V into Open Load Min. Step Voltage; 0.2V into Open Load**
- **Pulse current: 0-10 amps @ 50Ω load, 20 amps @ short circuit**
- **Pulse risetime: 100ps, 200ps, 400ps (built-in, software selectable)**
- **Pulse rate: ≈ 10 test pulses per minute**
- **DUT voltage sensor risetime: 30ps**
- **DUT current sensor risetime: 35ps**
- **Leakage voltage: 0 to 100v (0.1 v increments)**
- **Leakage current sensitivity: 1 pA to 2.5 mA**
- **Source impedance: 50Ω**
- **Load Impedance: any silicon ESD voltage clamp circuit**
- **Factory Selectable power: 100,120 vac@ 1.5amps; 220,240 vac@ .75amps, 50 to 60 Hz (USA default: 120 vac; 60 Hz)**

Features and Benefits

Accuracy

Special Barth wide bandwidth pulse current and voltage sensors provide a high standard of measurement capability for ESD test equipment. The complete system has been built with special attention paid to minimizing losses in the test circuitry and the coaxial cable connections. This results in accurate measurements of low dynamic resistance CDM protection circuits directly at the silicon pads.



Options and Accessories

External Parametric Tester Option
Allows connection of an external tester for more extensive characterization or functional testing of DUT in between pulse tests

BGA-TF Test Fixture – Model 40312
BGA-TF Test Fixture (includes one BGA probe)

RF Probe Head
RF Probe Head for use with either the Vacuum or Magnetic VFTLP+ Wafer Probe Positioner; (xxx= micron spacing).
Manufactured by Cascade Microtech®

VFTLP+ Wafer Probe Positioner, Magnetic
Manufactured by Cascade Microtech®

VFTLP+ Wafer Probe Positioner, Vacuum
Manufactured by Cascade Microtech®

Silver Shorting Pad - Silver Short with 15ea. 5.5Ω resistors on alumina base to allow a short calibration or verification of system

Data Storage

Data is automatically stored to hard disk in comma delimited format and can be recalled for viewing or transferring to disk. Data is automatically time/date stamped when saved.

Hardcopy Printout

Hardcopy printouts on a color printer listing data point values and showing plotted results using operator selected scaling are immediately available in a presentation ready format at the end of a test.

Size and Weight

System is 19”W x 11”H x 20.5” D (total height with a Tektronix Model DPO70604 is 21”). 147 lbs (not including external PC, monitor, or packing materials).

This Product Features Barth Designed ZAPLESS ® High Speed Measurement Components

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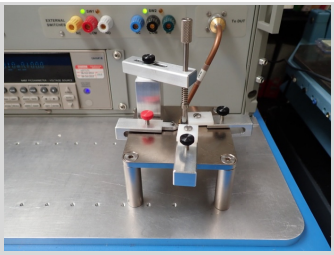
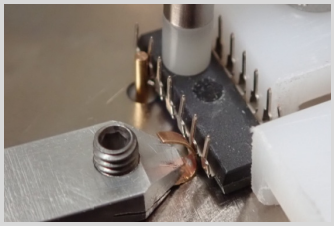
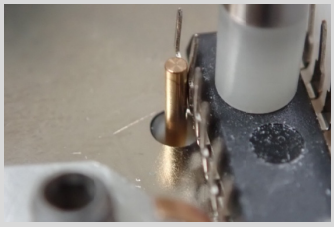
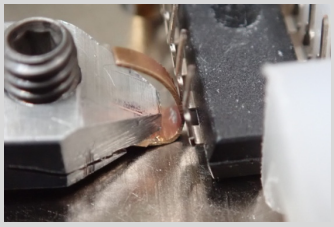
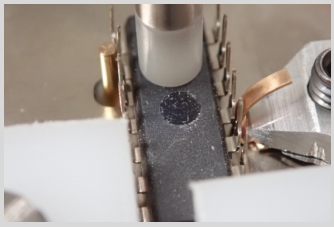
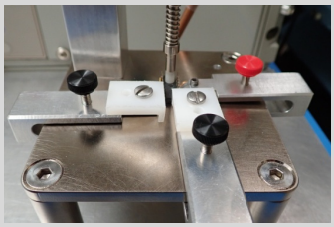


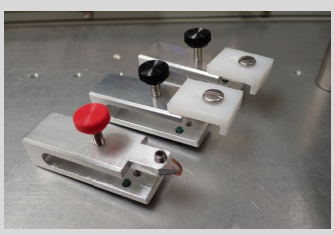




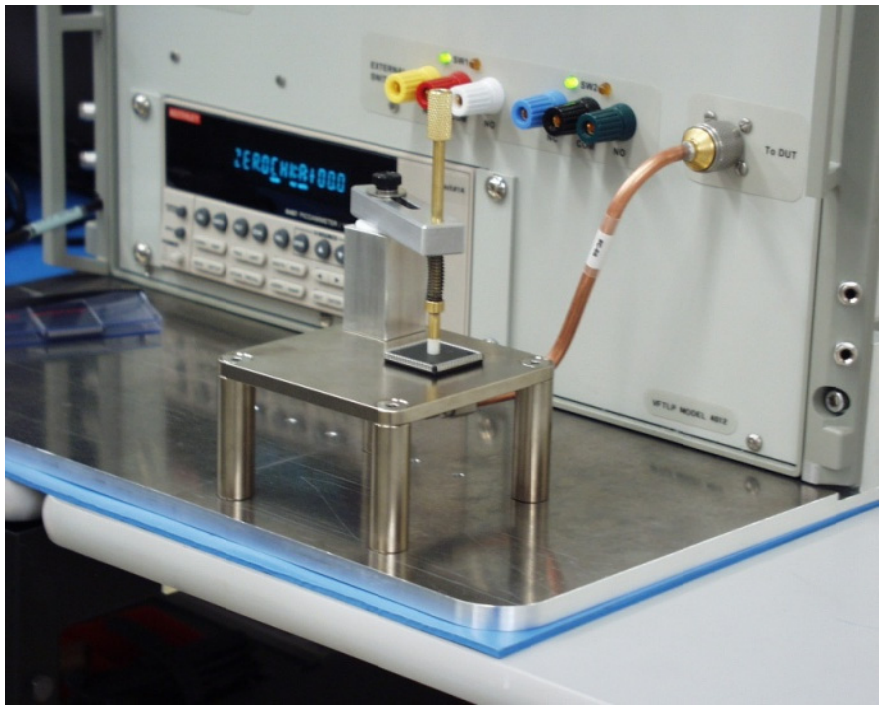








Universal Test Fixture - VFTLP
Barth Model 40212-UTF



The Universal Test Fixture is designed to be used with the Model 4012 VFTLP+ Test System for packaged part testing. A packaged DUT is placed dead-bug style on the ground plane, with the pin to be pulsed contacting the pin protruding from the base. The return pin is connected to the base through a special clamp to the baseplate. The vertical plunger and additional clamps insure the DUT is held in position.

The fixture can also be used for testing in a Capacitive Coupled VFTLP (CC-VFTLP) mode by not connecting a return (ground) connection. In this mode the system provides high pulse threat and current measurement into one pin of IC's to simulate the CDM threat. Because the DUT is lying on the test fixture ground plane, the measured current pulse waveform into any pin will be an exact replica of a real CDM event. A packaged DUT placed dead-bug style on the ground plane will provide the same capacitance at any pin to to ground as will occur during CDM testing. The leading edge of a 100 ps rise time rectangular pulse can then be applied to any pin on the DUT. The resulting charge type current into the circuit under test closely simulates the CDM test.

Leakage testing through the measurement connection allows the test pulse failure level to be constantly monitored in situ as the test pulse amplitude increases. High speed current measurements also identify the adding DUT capacitance and increased RC decay time as more circuits inside the package turn on. This test is designed to be used on packaged parts, after the silicon circuit has been designed with conventional wafer level testing on the Model 4012 VFTLP+ Test System.

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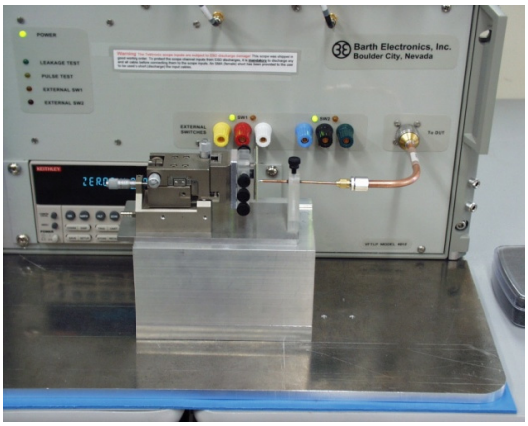
VFTLP+ BGA-TF Test Fixture
Barth Model 40312



The Model 4012 Very Fast TLP Plus (VFTLP+) system required 5 years to create a system which can simulate the CDM test in the time domain. This very fast hardware capture the fastest parts of the high speed waveforms never quantitatively identified before. The instrumentation developed for this system provides accurate waveform measurements of circuits needed for both a very fast pulse source and extremely fast response current and voltage sensors. In addition to the well-known I-V data used for analysis of electrical characteristics of ESD protection structures, the VFTLP+ system captures both voltage and current waveforms at the Device Under Test (DUT).

The BGA-TF Test Fixture is designed to be used with the VFTLP+ system. It provides high pulse current measurements of CDM type protection directly to two balls with minimum inductance without an expensive BGA high speed socket. With the DUT isolated about ground planes, there is no capacitance to ground effects on the current and voltage waveforms; measured directly at the package terminals.

While of limited value, this test is as close to the internal circuit operation as it is possible to achieve from the outside. This DUT fixture allows two pin testing to determine the amount of correlation with CDM.

To minimize the parasitic inductance from connections to the VFTLP+ system, this test will be most effective only when testing closely spaced balls. Metal and silicon failures from high currents at CDM pulse widths will be achieved; but internal GOX stress may not closely simulate the CDM test.

Metal/Silicon failure levels with this fixture combined with gate oxide failure levels using direct VFTLP+ failure measurements, can be combined to improve correlation with CDM. Continuous leakage monitoring through the measurement connection allows the test pulse failure level to be constantly monitored in between pulse measurements.

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Barth 4012 Application note #1

Revised 03/07/07

CDM Circuit Turn-On Analysis Using Very Fast TLP (VFTLP+) Waveforms

The 4012 Very Fast TLP (VFTLP+) system captures DUT voltage and current waveforms in addition to generating I/V data. The machine was built with the best possible hardware so that software could analyze and extract accurate data from these captured waveforms. This machine has the ability to capture and save waveforms for both the current through the DUT and the voltage across the DUT. The number of I-V waveforms displayed on the waveform screen is determined by the position of two cursors on the I-V plot screen. By moving each of the two cursors the user can display one or many DUT voltage and current waveforms.

The position of the pads for this test chip, required that we use the negative test pulse. Future software will allow the I-V data to be put into the first quadrant and display all waveforms as positive going for ease of visual analysis.

The I-V plot in Figure 1. shows three I-V characteristics of an excellent CDM protection circuit at different pulse widths. We made all three pulse width measurements on one CDM protection structure avoiding failure levels known from previous tests of identical test structures. The green data points are from the 1 ns long test pulse which didn't fail at the maximum test pulse amplitude which produced 18 amps at 17 volts in the DUT. The blue I-V data points from 2 ns pulse testing was terminated at about 12 Amps to avoid failure which occurs at about 16 amps. Because the 5 ns long test pulse was the last test on this structure it was taken to failure, which occurred at about 7 amps. This particular CDM test structure was very robust and provides an excellent demonstration of the capabilities of our 4012 VFTLP+ machine.

These structures had gate monitors to simulate the sensitive gate in the core being protected, and are the failure level indicators when leakage current increases. There is a way to make certain that the greatly increased leakage current was caused by gate monitor failure. If a retest of the test structure produces the same I-V characteristics, this indicates that the protection circuit was unchanged, and undamaged.

Failures current levels of devices at different pulse widths will be more thoroughly analyzed in the future. The ability of the VFTLP+ to provide actual DUT voltage amplitude waveforms into the core will allow more precise analysis of how gate oxide failures compare to Time Dependant Dielectric Breakdown measurements made with flat top pulses.

Measuring the same CDM test structure at three different pulse widths is useful because it shows how the circuit conductivity changes with shorter and longer pulses.

The 1 ns (blue), 2ns (red), and 5 ns (green) long test pulse I-V data shows how multiple I-V plots are displayed on the same screen.

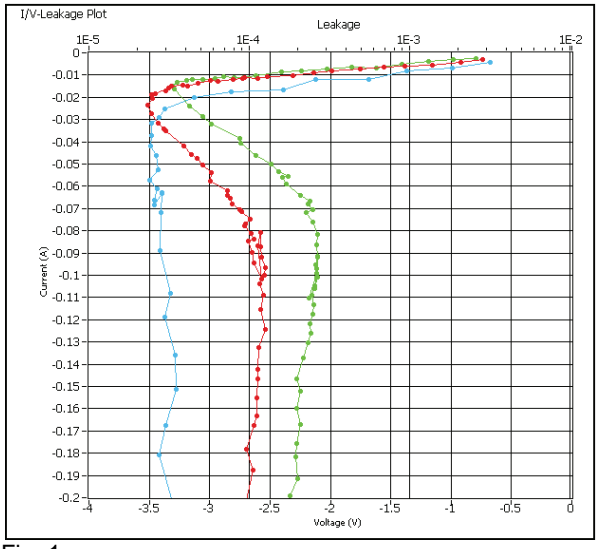


Fig. 1

The blue plot shows how the device turns on at 1 ns pulse width. The pulse is so short that the circuit doesn't have sufficient time to fully conduct into its snap-back mode. An approximate measure of the negative resistance at the slight snap-back conditions indicate that it would be about -0.60 ohms. This short pulse test shows that the circuit cannot get into its higher conduction made to cause the

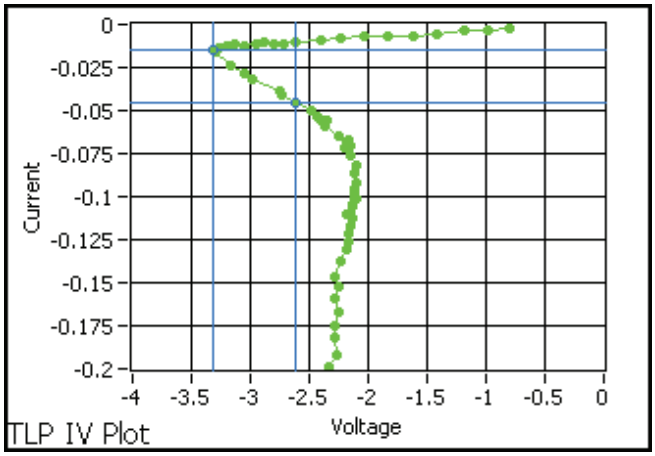
voltage decrease to amplitudes it will have when the test pulse is longer; but although the voltage remains higher throughout increasing current pulses, the shorter pulse width does not cause this gate monitor to fail at the maximum test pulse amplitude.

The red plot is made with the 2 ns long test pulse and shows the beginning of the snap-back operation. It shows a noticeable decrease in DUT voltage after snapback. Its snap-back negative resistance can now be measured at about -16.7 ohms.

The green plot is made with the 5 ns long test pulse and shows a more conductive snap-back operation that holds the voltage at even lower levels. The negative resistance during snap-back is now noticeably higher at -23 ohms. Again this test structure is an excellent example of a very well designed test structure that turns-on as desired for CDM protection.

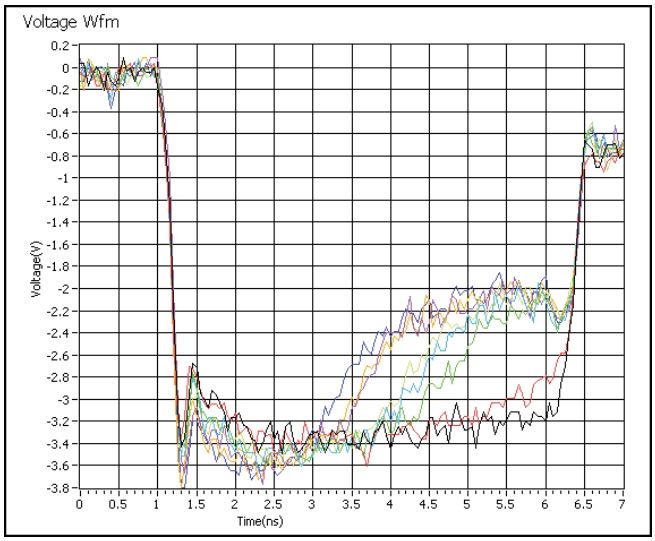
The user can display many different color plots on this screen but keeping them to 8 or 10 plots on one screen limits data confusion when the complete I-V range is displayed. When current and voltage scales are expanded, however, the difference between multiple plots becomes very clear. Subtle differences in multiple similar plots I-V plots can be clearly identified in this way. Although the noise levels in VSTLP increases above a few amps there is a significant advantage in data analysis when using a TLP systems with accurate measurements at all time ranges. Lower accuracy VFTLP systems will provide lower accuracy information on the differences between minor changes in ESD circuit design.

The green data points below form the I-V plot of the 5 ns long test pulse data in the low current region of a CDM circuit where turn-on begins.



The 4012 VFTLP+ software uses two blue cursors used to select two I-V data points which includes all the data points between them. The seven (7) green DUT data points select the all the voltage and current waveforms to be displayed on two more screens for analysis of turn-on characteristics.

The **voltage waveforms** below show a number of interesting facts.



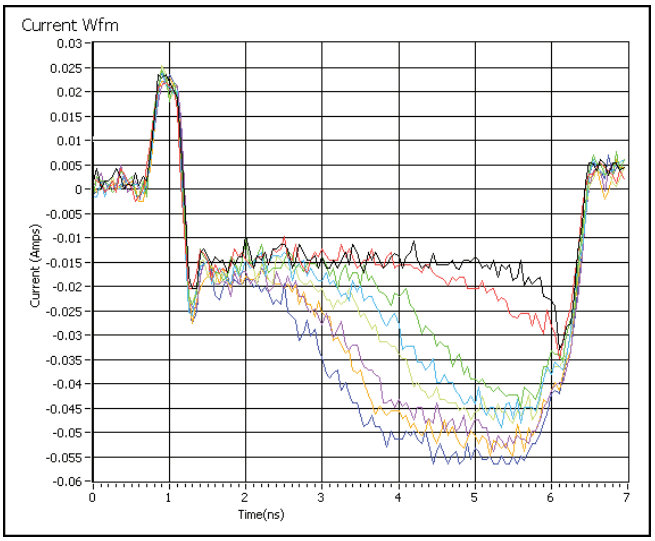
1. The lowest voltage data point is the black trace where it is relatively constant throughout the length of the five (5) nanosecond test pulse.

2. The second higher voltage waveform point is shown as red. It shows a slight decrease in voltage near the end of the 5 ns pulse as the circuit starts to conduct in a nonlinear fashion.

3. The next higher voltage waveform is shown in green. It also shows a significant decrease over the last nanosecond of the 5 ns long pulse.

4. The highest current point between the two green cursors on the I-V plot is shown in blue on both the DUT Voltage and Current plots. Here the voltage has started to decrease after about 3 ns and shows major voltage decrease during the last 1.5 ns of the 5 ns long test pulse. The current increase after a few nanoseconds occurs at the same time as the decreasing voltage.

The **current waveforms** between the two selection cursors are shown below.



1. Again the lowest test pulse amplitude is the black trace which is relatively constant throughout the length of the five (5) nanosecond test pulse.

2. The second higher current waveform is shown in red. It shows a slight increase in current near the end of the 5 ns pulse as the circuit starts to conduct in a nonlinear fashion.

3. The next higher current waveform is shown in green. It also shows a significant, linear increase over the last nanosecond of the 5 ns long pulse.

4. The highest current point between the two green cursors on the I-V plot is shown in blue on this DUT Current waveform. Here the current has started to increase after just 1 ns and shows a major linear current increase during the middle ns of the 5 ns long test pulse. The current increase after a few nanoseconds occurs at the same time as the decreasing voltage.

These are just seven waveforms for this particular CDM protection circuit during its interesting turn-on phase. The waveforms at all the higher currents with voltage and current amplitudes during the pulse are also available. Many more details beyond this cursory analysis will certainly be extracted from accurate waveforms, when studied by ESD designers.

One of our associates in ESD design commented that a Very Fast TLP (VFTLP+) system would not show any useful CDM design information. He must have forgotten the limited understanding of early TLP data, with the limited accuracy available from early crude machines. Today TLP data has such extreme value that all ESD design tutorials make specific demands that is must be used if efficient and good ESD protection is to be achieved.

Barth Electronics has complete confidence that intelligent ESD designers will devise methods to extract, and expand on the preliminary analysis of VFTLP+ waveforms made here. That is why we have invested so much time in developing the most accurate fast pulse hardware and waveform capture software for sub nanosecond time analysis of CDM protection circuits. Improvements in protection circuit design can grow rapidly when accurate sub-nanosecond voltage and current waveforms details are used.

An analysis of all the waveforms, at increasing amplitudes can now identify how the CDM protection circuit turns on during the test pulse time. Knowing the dynamic conductivity at each period of time can now provide the CDM designer with details impossible to measure previously. The data shown here was taken at 100 ps risetime. What additional design data may be able to be extracted from VFTLP+ data taken at slower risetimes of 200 and 400 ps?

Barth 4012 Application note #2

Introduction to VFTLP+

VFTLP was originally developed to provide I-V characteristics of CDM protection and its analysis has been similar to that of TLP data used to analyze HBM protection circuits. VFTLP and TLP data are an average of the voltage and current waveforms taken in the measurement window. TLP for HBM circuit analysis provides very reasonable average voltage and current data after their waveforms have settled down and are relatively constant.

HBM failures are primarily the result of energy dissipation in silicon protection elements. CDM threats are 1 to 2 ns long, while HBM treats are about 100 to 200 ns long. CDM is different from HBM in two important respects. First, CDM currents create voltages which are applied to gate oxides. Oxides fail when their voltage capability is exceeded.

The second major difference is that HBM testing specifies 2 to 10 ns current risetimes while the CDM event is extremely fast. Its risetime is as fast as 100 ps and the length of its pulses are much shorter. In order for VFTLP to simulate CDM events its test pulse risetimes be as fast as this 100 ps. The original VFTLP test system used shorter pulses with the intention of simulating CDM. However this test still uses the I-V data averaged in the measurement window. Although averaged data is useful in understanding the basic I-V characteristics of the CDM protection element, it misses time varying information. The high speed CDM event creates rapidly changing current and voltages in the silicon protection elements or circuits. Understanding their high speed response introduces a new and very important indicator of CDM protection circuit operation, that is impossible to identify using only current and voltage data averaged during a measurement window.

Because the primary cause of failure with CDM is gate oxide failure, voltage is the primary information needed to understand protection elements or circuits. The high speed CDM event creates very fast rates of current and voltage rise inside high speed IC's. We have developed special 30 ps risetime voltage and current sensors to identify the total DUT response with our VFTLP system. Measuring the high speed operation of silicon elements or circuits on wafer provides a new insight into previously un-known details of protection element operation.

Our VFTLP also adds true 100 ps risetime test pulse capability to simulate the CDM testing and CDM events. To deliver the high speed test pulse to the DUT, we always use very low loss transmission lines. Our very high speed wafer probes achieve extremely low inductance connections to the wafer. We identify this carefully engineered CDM circuit analysis tool as VFTLP+.

Our measurements of protection circuits on wafer have identified oxide threat Time Dependent Dielectric Breakdown (TDDB) voltages. Until now this measurement has been made with rectangular pulses to identify oxide voltage sensitivities to relatively short pulses. We have found that the first part of the oxide voltage threat is the initial voltage impulse. We identify this as the Initial Voltage Impulse (IVI) because it occurs in every VFTLP+ and CDM event. It is caused when extremely fast CDM events create very narrow voltage impulses, typically being 150 to 200 picoseconds wide. More complex protection circuits take additional time to turn-on and the IVI fall time can be as long as 5 ns. The IVI precedes the average steady state voltage identified in the measurement window. The IVI voltage has been referred to in previous papers although the true peak voltage has not been available. With both limited risetime test pulses and limited DUT response risetime measurement systems, the real silicon IVI cannot be determined.

The total oxide threat can now be identified by measurements of the voltage created by silicon protection circuits during the total time the threat is applied.

Diodes are a common element used for CDM protection. To demonstrate how voltage developed across a protection element varies during the test, we measured some micro-miniature silicon signal diodes. These diodes are only one mm long and have very low package inductance. The inductance is low enough that it does not become noticeable until the VFTLP+ current increases to a level high enough to increase the L/R effect. At this time the voltage impulse from –L·di/dt effects become visible. We identify this as the Secondary Voltage Impulse (SVI) because the negative polarity inductive voltage "kick" from fast risetime current flowing though an inductance occurs when chips are packaged.

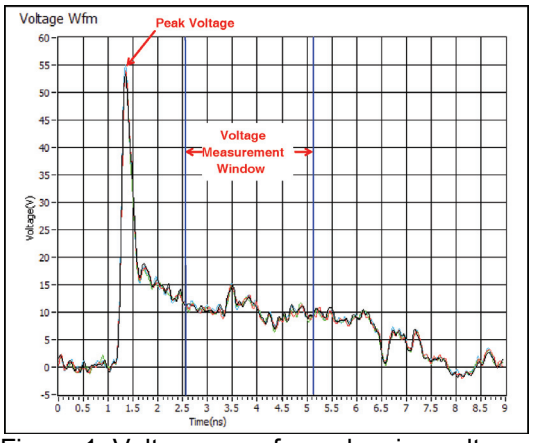


Figure 1. Voltage waveform showing voltage averaged over the measurement window and peak value

Semiconductors have an inherent delay between the time a voltage is applied and the current flow completes the silicon path. Our VFTLP+ system has permitted us to investigate high speed physics of semiconductors. The time delay between the application of voltage and carriers completing their path through silicon is typically identified as being 10 to 20 picoseconds. This time delay is dependent on the path length through the semiconductor and the applied voltage. Higher voltages increase the speed of carriers in semiconductors until the saturation velocity limit is reached.

These introductory measurements of commercial diodes were made on 1N4148 diodes soldered directly to the end of a time calibrated piece of 0.085 inch diameter semi-rigid coaxial cable. The cable is connected to the VFTLP+ tester with an integral SMA connector. Great care must be made to assure that the measurement reference location is positioned at the end of the coaxial test cable where the DUT is located. These measurements can be made with any VFTLP machine on similar diodes. Accurate information on the voltage overshoot which occurs before the current carriers complete the circuit path through the silicon must be made with 100 ps risetime. Simulating the CDM event is of paramount importance if VFTLP is to provide its inherent capability.

Diode Turn-on Time Measurements

Note: The first measurements made of the 1N4148 miniature size package were made at the end of the two wires, which extend about 0.095 inch past the end of the 0.085" dia. copper jacket.

We also made tests of the inductance of these two wires by placing a 0.040 wire short between them 0.070" from the body to simulate the 1N4148 diode position. These relatively short wires extending out from the coaxial cable added a significant amount of inductance.

To remove as much lead inductance as possible we connected the much shorter leads in micro-miniature 1N4448 diodes directly at the end of the Teflon. It was placed between the 50 ohm inner conductor and its Copper jacket. Removing the wire leads and moving the diode 0.095 inch closer to the timing short reference end of the coaxial cable shows noticeably less inductance.

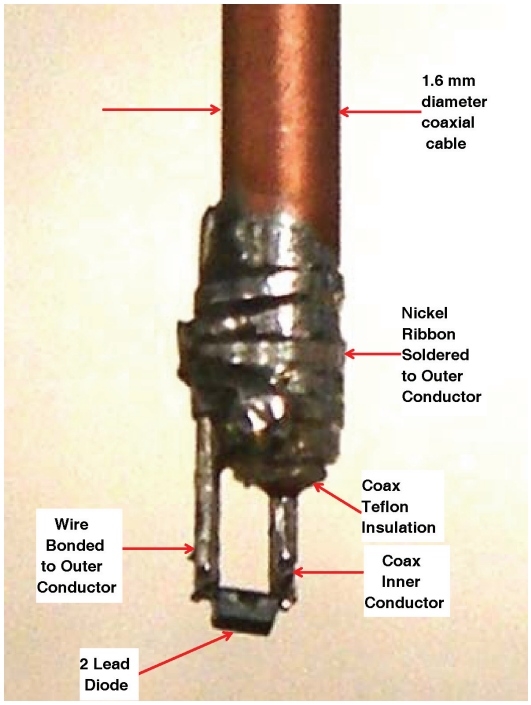


Figure 2. 1N4148 diode mounted on coax

This second diode has the shortest total package lead length and therefore has much less inductance. It is a Digi-key part number MMBD4448HTADICT-ND. The manufacturer's part number is MMBD4448HTA-7. It is in a SOT-523, 3 lead packages but only one of the two diodes in the packages are used. It is rated at 80V; and 150 mW. Measurements of this small diode positioned directly at the zero time location of the DUT coaxial cable, minimizes the parasitic lead inductance. When measuring packaged parts, the leads out side the package can be made short, but the lead frame and bond-wires to the chip add measurable inductance. The total inductance creates a significant -L·di/dt voltage impulse at the beginning and end of the test pulse. This voltage impulse is added to the Initial Voltage Impulse (IVI) of the semiconductor makes the exact time delay difficult to establish.

These first examples are used to emphasize the rate of silicon conductivity increase possible to measure with fast rising test pulses on commercial diodes. The voltage IVI and the rate of current increase are similar to some CDM protection circuits which use SCR elements.

The first voltage waveform in Figure 3 (black trace) is at about 1 volt and draws no current for the same trace in Figure 4. The voltage is constant at 1 volt. The second test pulse is about 2.5 volts (red) and remains at that level for about 1.5 ns; then begins to decrease to the 1 volt constant silicon conductivity level in 3 or 4 nanoseconds. The 100 ps risetime test pulse creates the high amplitude voltage across the diode. The peak voltage created when using slower risetime test pulses of 200 and 400 picoseconds create lower peak voltages. These large diodes provide excellent examples of the slowly increase in silicon conductivity. After they reach the peak voltage they begin an immediate but slow decrease toward 1 volt over a similar 3 to 4 nanoseconds time period.

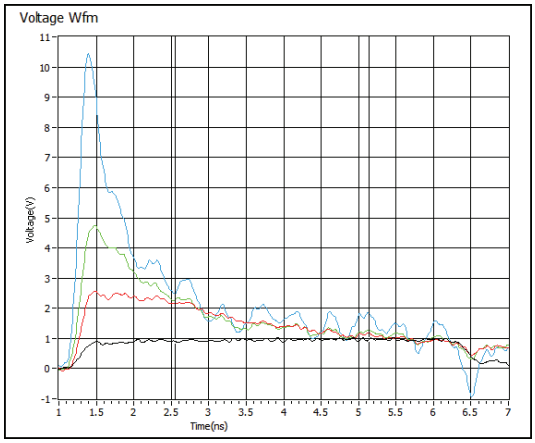


Figure 3. Voltage waveforms of 1N4448 diode

There is no current created when the 1 volt test pulse is applied to the diode, as shown in the black trace. The slow increase in current is obvious in the next test pulse (red) as the current requires almost 4 nanoseconds to reach its constant amplitude.

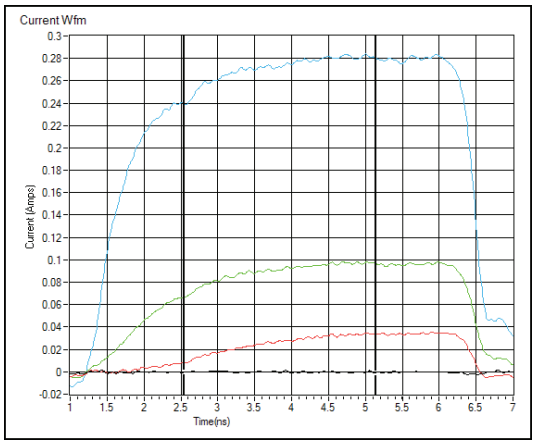


Figure 4. Current waveforms of 1N4448 diode from 0 to 0.27 amps

At higher pulse currents the dynamic resistance of the diode becomes lower and increases the –L·di/dt IVI effect. This is shown for higher amplitude pulses as the pulse voltage increases, creating higher currents (green, and then blue). Higher test pulse voltages cause the carriers to move more rapidly and the steady state current is reached more rapidly until carrier velocity reaches saturation.

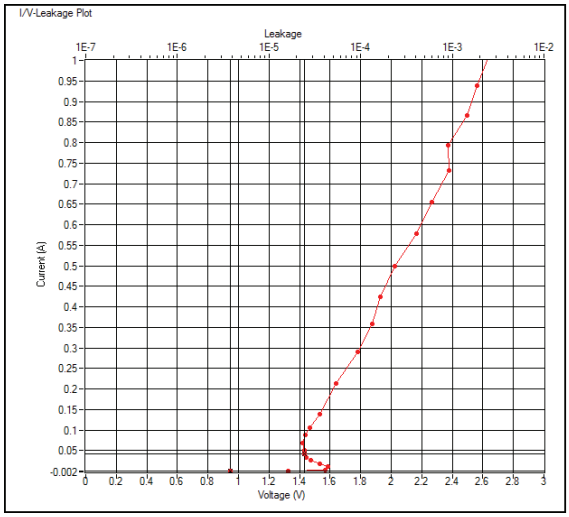


Figure 5. Snap-back suggested by this I-V plot of an ordinary diode.

By examining the voltage waveforms below in Figure 6, we can see that the Initial Voltage Impulse is immediately followed by decreasing voltage. The measurement window indicated by the heavy black lines at 2.5 ns and 5.1 ns shows the average (Vt1) of the decaying voltage being less than the peak voltage of about 2 volts.

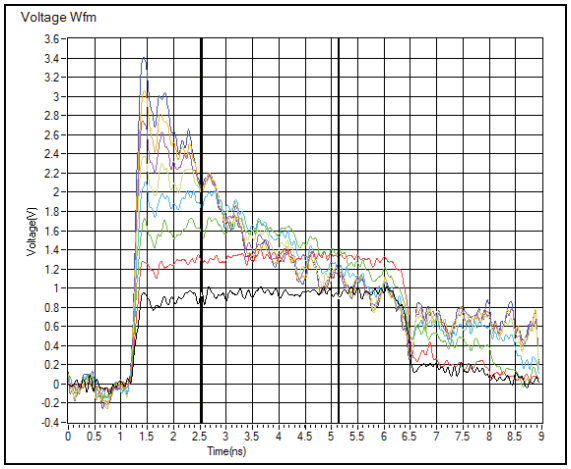


Figure 6. Voltage waveforms measured over 0 to 1 amp range. For clarity only every third waveform is shown.

By replacing the diode package with a conductor having the same dimensions as the diode package leads, the –L·di/dt voltage impulses at the beginning and end of the test pulse can be identified. This is only approximate however, because the physical dimensions of the bond wire from the lead frame to the chip inside the package are only estimated.

Measurement Window Location?

The plot in Figure 5 would normally indicate a snapback element. However the diode we are testing does not exhibit a snapback characteristic.

The waveforms show that the voltage is not a snap-back condition. Because the average voltage in the measurement window is temporarily lower than the average of earlier test pulse voltages, an average measurement gives a false indication of snap-back.

Measurements of the 1N4448 diode were made with a 5 ns long pulse. As shown in figure 6, the first three test pulses produce very low current and immediately fall to zero at the end of the pulse.

At higher amplitude test pulses the voltage and current are seen to continue after the end of the 5 ns long test pulse. This is the stored charge effect in the diode. Depending on the silicon protection element characteristics, this voltage sometimes continues at a significant amplitude. This can add voltage for some part of a nanosecond to the TDDB threat. If the length of time a voltage is unexpectedly extended across a gate oxide, during either VFTLP or CDM test pulses, GOX failures can be lower than expected.

To display both the average and peak voltage we introduce the dual voltage plot shown below in Figure 7. It displays the total voltage threat very clearly by adding the peak voltage to the usual VFTLP I-V average current and voltage plot shown in Figure 5 above.

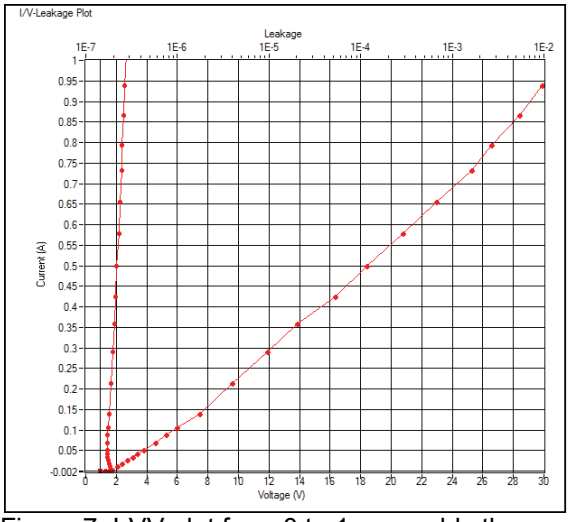


Figure 7. I-VV plot from 0 to 1 amp adds the peak voltage measurements to the standard VFTLP Plot .

The total voltage threat in a single display provides a simple but effective graphical presentation. The ordinary I-V data in this plot is the same as that shown in Figure 5.

By adding the peak voltage to the I-V plot, both threats produced by CDM protection circuits can be rapidly analyzed.

We identify this as an I-VV plot because both the average and peak voltage are measured and graphically displayed.

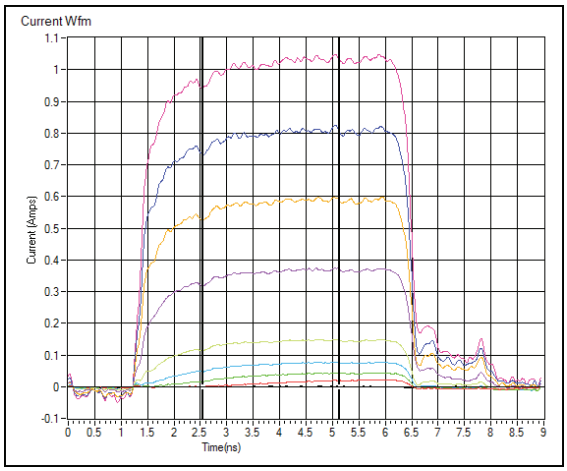


Figure 8. Current waveforms from 0-1A

This figure shows the current waveforms increasing more rapidly as the test pulse amplitude increases. Increasing test pulse voltages increase the speed of the carriers through the silicon element. The large path length in the individual diodes tested here creates a longer path than is found in ESD protection elements. Therefore the IVI in simple ESD diodes is much lower; however more complex ESD protection elements such as an SCR can have very similar rates of voltage decay with very high peak voltages.

Conclusions

The ability to simulate CDM rates of rise and measure its effect on silicon protection circuits is provided in the VFTLP**+** test. While we measured diodes larger than those used in ESD protection, it demonstrates the high speed measurement capabilities needed to understand the high speed operation of silicon. Commercial diodes such as the ones we tested do not fail at the highest pulse current and longest pulses. They are readily available and their time delay characteristics are very repeatable.

Barth 4012 Application note #2

The waveform and I-VV plot data provided by this VFTLP**+** test adds completely new analysis to the original VFTLP system. Improving CDM protection is important because the sensitivity of gate oxides continues to increase.

We are eagerly searching to test CDM protection on wafers. This new analysis tool can provide an important data base for ESD design. This information will be the first time manufacturers of wafers will be able to see the complete protection element characteristics at the high speeds which simulate the CDM test.

The wafer information we measure and publish will be isolated from other manufacturers, because this type data has never been published previously. We need to measure more silicon elements or circuits on wafer to assemble VFTLP**+** information as an introduction for the industry.

This data is the first of our application notes for this VFTLP+ test system. Those who supply wafers for this testing will be the first to receive full information time history on their CDM protection design details and the effects geometry variations have on gate oxide failures.

We will continue to publish application notes to develop a better understanding of circuit response to high speed threats. This test method can begin a correlation between voltage response and variations in geometry. Voltage and current waveforms on future silicon CDM protection will become more analytical as dimensional details are better understood.

We can provide this information to begin a better understanding of previously hidden operational parameters of high speed ESD protection.

This first presentation demonstrates how ordinary VFTLP has been improved to expand design data it is now possible to extract from CDM protection elements. We have devoted over two years to this test system and will continue to expand the value of this new analysis tool.

Our measurements of actual CDM protection circuits and individual test structures data will continue in future application notes. The generosity of potential customers, in providing silicon protection elements on wafer has been most helpful in understanding the basics of high speed silicon protection. The small amount of data we have recently measured provided the basic requirements needed for CDM design. This new source of data begins a new ability to analyze the high speed operation of silicon elements and circuits in continuous time detail.

Jon Barth
Chief Engineer
Barth Electronics, Inc.

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RELYING ON BARTH ESD TEST SYSTEMS

Ampleon	1	New Japan Radio	1
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Borg Warner	1	Qualcomm	1	1	1	1	1
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Chartered Semi	1	Rohm	1
Cirrus Logic	1	Sandia	1
Cypress	1	Samsung	1
Denso	1	Semtech	1	1	1	1	1	1
Diodes Inc.	1	1	Sharp	1
Dongbu - Anam	1	Silan	1
Defense Microelectronics	1	Silanna	1
Eurofins	1	Silicon Labs	1	1	1
Fairchild Semi	1	1	Sino-Tech, China	1
Fujitsu	1	Skyworks	1
Global Foundries	1	1	SIMTech	1
Huawei	1	SMIC	1
HeJian	1	Sofics	1	1	1
HHNEC	1	Sony	1	1
Honeywell	1	ST-Tours	1
Hong Kong Applied Sci.	1	Synaptics	1	1
Hynix	1	TA-I	1
IDT	1	TET	1
Intel	1	1	Texas Instruments	1	1	1	1	1
Intersil	1	- TI Cont'd.	1	1	1
Lexmark	1	Toshiba	1
Macronix (MXIC)	1	TSMC	1
Magnachip	1	U-blox	1
Maxim	1	UC Riverside	1	1
Microchip Tech	1	1	1	UMC	1
Micron	1	1	1	1	Univ. of Central FL	1	1
Mitsubishi	1	Vanguard	1
Monolithic Pwr Sys	1	Winbond	1
NXP	1	1	1	Zhejiang University	1

1 = One TLP+ Test System 1 = One VFTLP+ Test System 1 = One HMM+ Test System 1 = One CMT Test System

Common Mode Transient (CMT) Generator
Barth Model 781

3.12 To 1600 kV/µs Into 50 Ω Loads

Features:

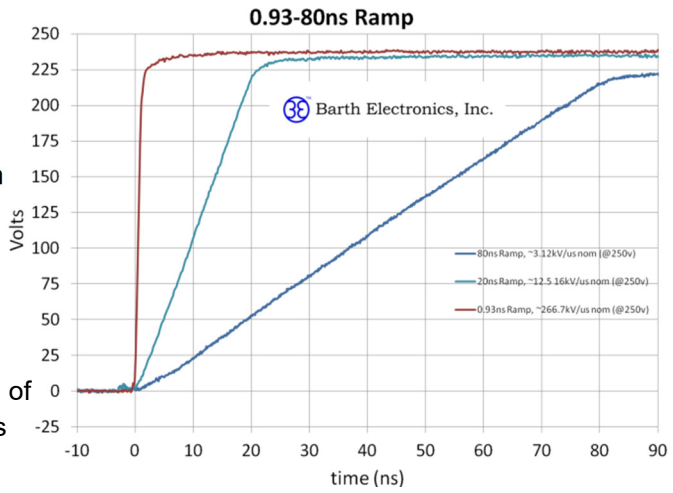
- Interactive control allows the user to gradually increase, or decrease the dV/dt rate applied to a DUT
- Stepped mode features user adjustable constant voltage and 14 stepped dV/dt selections
- Variable dV/dt mode features a more continuously variable dV/dt selectable by the user.
- 3.12 to 1600kV/µs can be delivered into 50 ohm loads
- 6.25 to 3200kV/µs can be realized into high impedance loads.
- Touch screen interface allows quick interactive and intuitive control.
- Internal rate and external triggering capability
- Designed for Common-Mode Transient Immunity (CMTI) testing
- Optional Exponential decay Pulse shape module with 50 ohm termination
- Provision for external switch Interlock
- One year warranty on the entire system

Description:

The Barth Common Mode Transient (CMT) Generator was developed for CMTI (CMT Immunity) characterization testing. The generator test system combines our 3kV Pulse Generator and Barth Multi Ramp Generator to produce high voltage, selectable fixed rate linear rise ramp pulses.

How It Works

The Barth Model 781 3kV High Voltage Pulse Generator produces a fast rise time high voltage rectangular pulse. This pulse is then passed through an internal Barth Multi Ramp generator module to create a linear ramp.

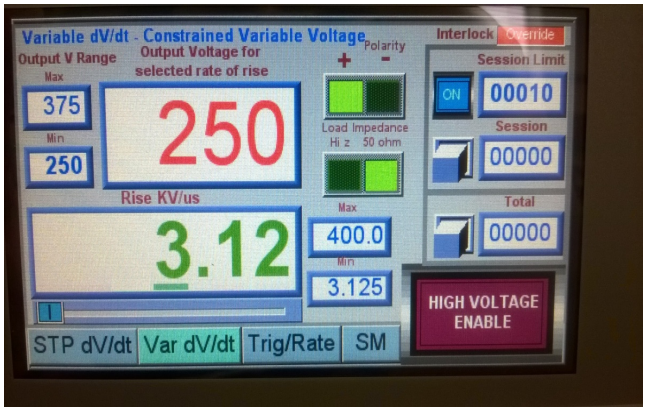


Samples of 0.93ns, 20ns, and 80ns ramp output showing Leading edge of pulse into matched 50 ohm load

Operation

Quick interactive and intuitive control of the generator operational parameters is provided via a touch screen interface. The test system provides interactive control of the two variables that define the dV/dt rate, the pulse voltage and ramp rate, to achieve specific kV/us rate pulses. The control also allows the user to interactively increase, or decrease the dV/dt rate which is applied to the DUT.

The 2 basic operational modes are: The “STP” stepped mode which features user adjustable voltage and 14 stepped dV/dt selections based on the 14 fixed ramp rates, and the “VAR” variable dV/dt mode which features a more continuously variable dV/dt selectable by the user. This mode is accomplished by varying the output voltage within an output voltage range and jumping to the next ramp selection as required automatically.



“VAR” variable dV/dt mode shown features a continuously variable dV/dt selectable by the user.

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Fax 702.293.7024
www.BarthElectronics.com

Common Mode Transient (CMT) Generator
Barth Model 781

System Components:

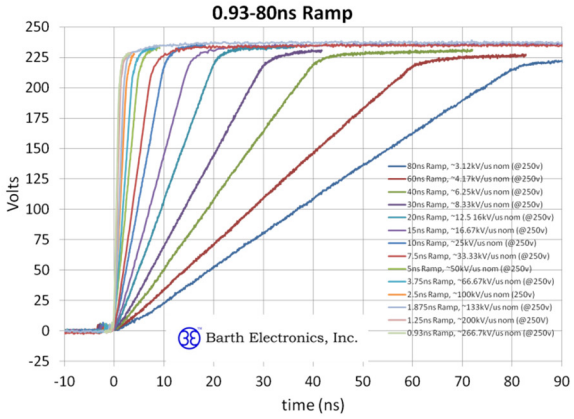
- Barth 781 High Voltage Fast Rise Time Pulse Generator
- 100ns Pulse Charge line
- Output cable Signal tap-off interconnect cables
- Optional Exponential decay Pulse shape module with 50 ohm termination

Specifications:

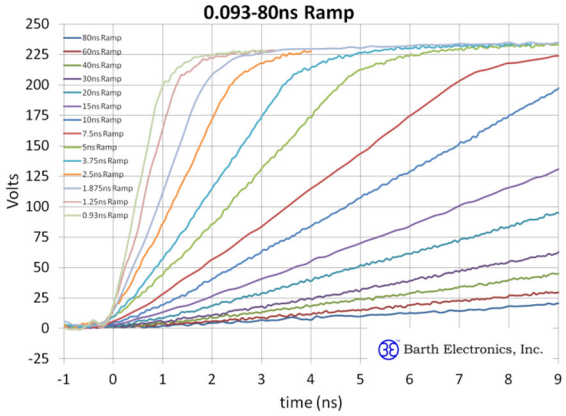
- 3.12 to 1600kV/µs can be delivered into 50 ohm loads
- 6.25 to 3200kV/µs can be realized into high impedance loads.
- 'N' Female output Connector.
- 90V-230V, A Input Power.

Size/Weight:

- Approximately 19" w x 11" h x 21"d.
- Total weight is approximately 55 lbs.
- Output compliant with IEC….specifications.



Sample pulse outputs showing Leading edge of pulse into matched 50 ohm load for all 14 ramp selections.

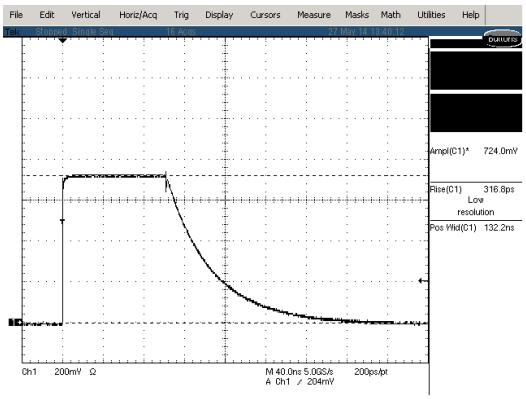


Same Sample Pulse Outputs with expanded time scale.

Operation (cont.)

Specific kV/µs rate pulses between 3.12 and 1600kV/µs can be achieved into 50 ohm loads. Rates between 6.25 and 3200kV/µs can be realized into high impedance loads.

The fall time mirrors the rise time, and with optional pulse shape module a long exponential decay fall time is also available as shown below.



Fast Ramp with Pulse Shape module (adds Exponential decay on falling edge) into matched 50 ohm load.

This Product Features Barth Designed ZAPLESS ® High Speed Measurement Components

Pulse Rate and Triggering:

The pulse rate and triggering is similar to the 731/733 pulse generator, including internal triggering for single shot or repetitive pulsing. Repetition rates to 10Hz are selectable. External triggering capability is also included.

Interlock:

The interlock provision provides a means to prevent pulsing when a test fixture with a lid or other movable safety is employed. This requires a switch on the fixture that will close to indicate the closed lid position.

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No Gun IEC Device Testing
Model 4702 IEC-50

Eliminate gun testing problems
No large gun tip
No separate Ground Return Cable
No special test setup with Coupling Planes

No excess gun radiation
Easy, repeatable connection to Device Testing Fixture Boards

Direct probes to pads for Wafer Level Testing
Optional wafer probes and cable available

Complete testing in one step
Direct cable connections to DUT, leakage test after each test pulse, computer controlled test level steps for automated testing

Verifiable testing
All current pulses recorded from oscilloscope

The ESD gun has now been replaced by a stationary, computer controlled source feeding the IEC test pulse into a coaxial cable. Now, instead of moving the gun from point to point, the pulse itself is directed from the test pulse point to test point through a switching matrix.

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50Ω IEC Pulse Test System
Barth Model 4702 HMM+ ™

Preliminary Specifications:

Output to DUT (program driven)

- Pulse Rise Time: 0.7 - 1.0 ns
- I_{PEAK}: 3.75 A/kV* +/-10%
- I_{30ns}: 2.0 A/kV* +/-20%
- I_{60ns}: 1.0 A/kV* +/-20%
- Voltage Range: 500V-27kV*
- Max Current: 100A PEAK; = IEC gun current @ 27kV
- Pulse Rate: ~10 test pulse series per minute
- Leakage Voltage: 0V to 100V in 0.1V increments
- Source Impedance: 50Ω
- Load Impedance: Any load
- Size: 19”W x 20.5”D x 11”H control unit, 18”H includes Tektronix oscilloscope
- Weight: ~130lbs total system weight plus shipping materials

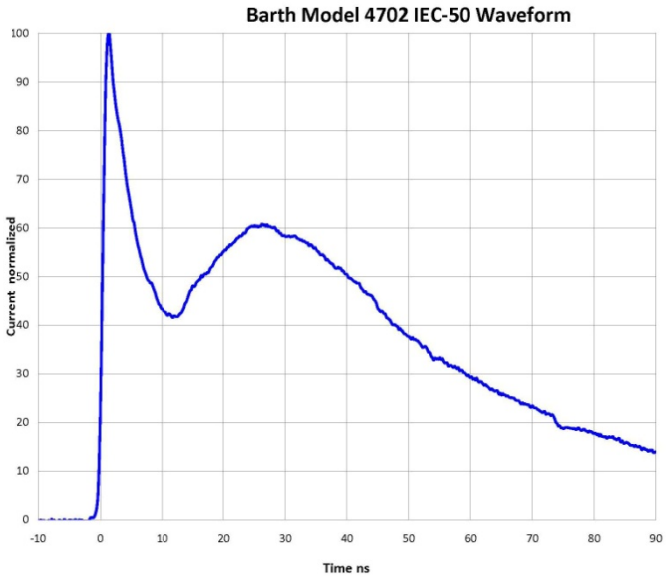
*IEC Equivalent Voltage

The Barth Model 4702 HMM+ ™ 50 Ω HMM Pulse Test System was designed and built to eliminate the common problems that are found with IEC gun testing. Gone are the interfering electromagnetic pulses that are induced with gun testing, and the system removes other undesirable effects that result from the gun’s separate ground return cable. The test system also solves the large gun tip interconnect issues, providing a very easy connection to test fixture boards.

Connection and Operation

Tester is connected to the DUT with a single 50Ω coax which delivers the IEC-HMM pulse and provides connection for leakage measurements in between IEC stress pulses. This method provides a ready and convenient connection for both system type and component level IEC testing. Wafer level testing is also supported.

Testing is computer controlled, allowing the user to gradually increase the HMM delivered threat, while checking the DUT leakage, measured in between threat pulses, to develop information on DUT failure levels and signatures. will include references to this 50 ohm source test method. The IEC pulse is defined by the basic immunity test method for personal ESD Specification, IEC 61000-4-2:2008. A new version of this standard is currently under development and will include references to this 50 ohm source test method.



Pulse voltage and current delivered to the DUT are measured with custom Barth wide bandwidth voltage and current probes for accurate waveform measurement. Waveforms are digitized and downloaded to the control PC for processing. Our measurements provide the ESD chip designer with the detailed waveform information, which allows for assessment of effectiveness of the ESD protection circuitry, and to verify compliance to the desired ESD immunity level.

This Product Features
Barth Designed ZAPLESS ®
High Speed Measurement Components

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50Ω IEC Pulse Test System
Barth Model 4702 HMM+ ™

HMM+ Pulse Test System Options

Computer Upgrade
(Replacement Computer for Existing Systems)

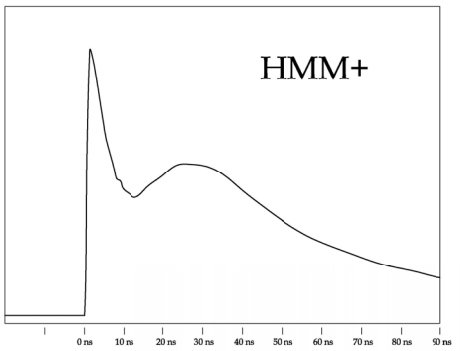
BCCU-4702

Includes a Dell Precision Work Station, 19” Monitor, WIN 10, National Instruments Interface Control Board: NI PCIE-GPIB w/NI-488 Software, 3 year Dell Pro Support Warranty on Computer, Software Upgrade, Barth Software Subscription Plan Includes 1 year BSSP

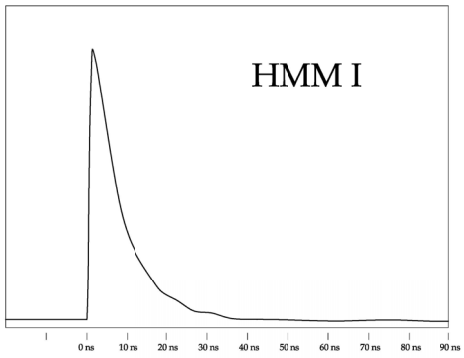
HMM +I/-I Option - Model 4702-02

The HMM +I/-I option provides the capability to also test your device with just the fast rise impulse threat portion of the HMM waveform, or just the slow rise wider pulse, energy threat portion of the HMM waveform.

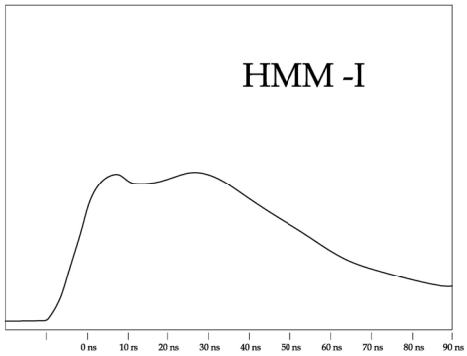
Testing of your devices with these different type threats provides you with additional information allowing you to better understand actual performance of specific portions of your design, allowing you to more quickly quantify performance and pinpoint potential issues with your protection structures.



HMM+ ; Standard HMM waveform



HMM I ; Impulse only waveform - contains only the high speed "impulse" portion of the HMM waveform threat



HMM-I ; minus impulse waveform-contains only the slow rise time "Energy" portion of the HMM waveform threat

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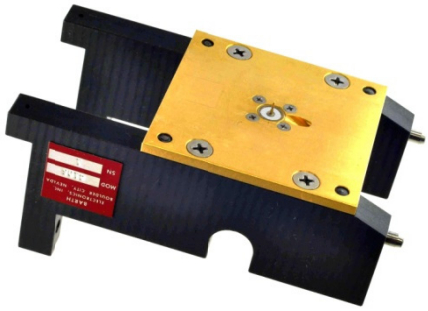
Wide Bandwidth RCDM-3 Current Sensor
Barth Model 4106

Features:

- Designed to be used with the RCDM-3 Test systems
- Supports use of wide bandwidth scopes.
- Addresses the need for accurate, repeatable measurements
- Enables comparable measurements from tester to tester



The Barth Model 4106 CDM current Sensor is designed to be used with the RCDM-3 Test Systems to improve the quality of measurements, especially when used with greater than 1GHz bandwidth scopes.

Specifications:

A/V Sensitivity variation: -0.2 dB/+0.6dB 500 to 3000 MHz

Resistive Impedance: 1.0 ohm +/- 0.3 ohm 500 to 3000 MHz.

Meets Current JS-002 and Q100-011 Specifications

User Replaceable Pogo Pin: Barth Model 410602

Improve Your Test Accuracy and Repeatability

The 20 year wait for improvements in CDM test accuracy and repeatability between testers is over. We at Barth have used our experience in producing high speed measurement components to design a new current sensor with uniform frequency response.

Many years after identifying the primary cause of CDM repeatability error, expectations that manufacturers would provide better measurement components remained unanswered. Our long term goal was to improve CDM data measurement correlation between all RCDM3 testers with individually calibrated current sensors. Adding tight specifications to the CDM standard will insure that data measured with 3 GHz or higher bandwidth scopes will produce accurate data that the industry requires.

Our work on these products began with detailed time and frequency domain measurements of existing CDM components. Our analysis determined that the existing time domain specifications ignore frequency parameters necessary for accurate measurements of actual CDM discharges. Holding tight tolerance specifications in the CDM discharge frequency range allows our Model 4106 current sensor to provide a new level of data accuracy. When all RCDM3 test systems produce accurate data, these new components in turn will automatically provide repeatable and comparable test data. Tight specifications for this current sensor frequency response and a true one ohm discharge resistance will lead the way to improved repeatability and accurate device failure levels.

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CDM Triple Verification Module
Barth Model 4181A

CDM Triple Verification Module for Calibration of RCDM-3 Sensors

Complimentary Accessories:

- Designed to be used with the RCDM-3 Test systems
- Module includes three (3) verification values for quick system verification.
- Indexed module alignment allows storing x-y location for quick discharge pin alignment.
- Supports use of wide bandwidth scopes.
- Addresses the need for accurate, repeatable measurements
- Enables comparable measurements from tester to tester

The Barth Model 4181A Triple Verification Module accessory is designed to be used with the Barth Model 4106 CDM current Sensor for the RCDM-3 Test systems to improve the quality of measurements, especially when used with greater than 1GHz bandwidth scopes.

Its low profile design allow it to be used without removal of the FR-4 base making calibration verification easy and convenient.

Specifications:

Capacitance values:	55 pF +/- 0.2% + 0.2 pF 6.8 pF +/- 1% + 0.2 pF 1.0 pF +/- 0.2% + 0.2 pF
Temperature stability:	+/- 0.1% 50°F to 120°F (10°C to 49°C)
Dielectric stability:	<0.01%, 5% to 95% humidity (40°F to 100°F, 4°C to 38°C) dew point.
Capacitance Variation:	< 1% DC to 3 GHz
Dielectric Loss Variation:	< 0.0003 DC to 3 GHz

Improve your test Accuracy and Repeatability

Barth introduces a new precision verification module for the RCDM3 tester in a convenient package for quick alignment and use. This new triple verification module provides an accurate and stable discharge source as an accessory for our Model 4106 current sensor.

The new verification modules use >99% alumina ceramic dielectric to eliminate the variable parameters of the presently used FR4 capacitor dielectric. We determined FR4 to be completely unsuitable as reference capacitors when improved accuracy measurement components are available. Alumina eliminates the variable discharge parameters of the FR4 hygroscopic effects, its variations with frequency, and its excessive high frequency loss properties. The triple verification module also eliminates additional variables caused by air gap differences with each placement. The results of these variations have been mostly hidden by inconsistencies in the original CDM measurement components and specified methods.

The new construction with greatly improved dielectric material makes this triple verification module a simple, but very effective, CDM tester verification source that will be part of the overall improvement possible with the Barth Model 4106 wide bandwidth current sensor.

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ORDERING INFORMATION

BUSINESS HOURS

We are located in Boulder City, NV, USA in the Pacific Time Zone. Our business hours are 8:00 a.m. to 4:00 p.m. Monday through Friday.

TERMS

Prices and discounts are subject to change without notice. Specifications for any product may be improved at any time without notice. Major improvements in a specification usually add a letter to the original part number.

Terms are Net 30 days. Accounts over 30 days are considered past due and will receive a finance charge of 0.05% per day (18 % per Annum). All prices are F.O.B. Boulder City, Nevada. We provide commercial packaging for shipment.

CONDITIONS OF SALE

Determination of price, terms, conditions of sale, and final acceptance of orders are made at the factory in Boulder City, Nevada.

DOMESTIC SHIPPING / RUSH ORDERS

Products in stock are available for immediate delivery. Every effort is made to stock the most popular items. Delivery for a product not in-stock is dependent upon our production schedule.

EXPORT TERMS / SHIPPING

The "end-use" and "customer name" for exported products must be included with all confirming purchase orders. Export orders may require a letter of credit or pre-payment, before order is shipped. If an export license is required; order processing and shipping may be delayed.

CREDIT CARDS

Barth Electronics, Inc. accepts VISA, Discover and MasterCard. Maximum credit card charge is $10,000.00 USD, per transaction. There will be a 4% processing fee added to all credit card orders.

DISCOUNTS

Discounts for quantities are available. Call factory for quantity discount pricing.

WARRANTY INFORMATION

We stand behind every high quality product we manufacture. Our commitment to quality and workmanship are among the highest in the world. Quality does cost and all high voltage pulse power items produced by Barth Electronics Inc. are buy it once use it forever, *when used within catalog specifications*. **Note:** Tampering of any Barth pulse product in *any way* will void the warranty.

DOMESTIC & INTERNATIONAL SALES

Contact the Barth sales team beisales@barthelectronics.com 1-702-293-1576, or visit our website for the most complete and up to date sales representative information at www.BarthElectronics.com

TECHNICAL QUESTIONS

For technical support email beitechsupport@barthelectronics.com , or call 1-702-293-1576

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